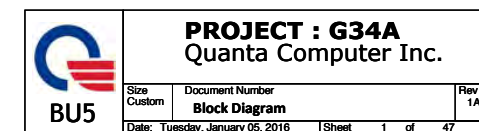


LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



+3V [4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47]
+1.0V [4,5,16,33,38]
+VCCSTPLL [4,5,6,9,38,39]

HDMI

[27] IN_D2#
[27] IN_D2
[27] IN_D1#
[27] IN_D1
[27] IN_D0#
[27] IN_D0
[27] IN_CLK#
[27] IN_CLK

U1A

SKL_ULT ?

Need apply PN

need surport to UHD 3840x2160

E55 IN_D2#
F55 IN_D2
F58 IN_D1#
F53 IN_D1
G53 IN_D0#
F56 IN_D0
G56 IN_CLK#
G56 IN_CLK

DDI1_TXN[0]
DDI1_TXP[0]
DDI1_TXN[1]
DDI1_TXP[1]
DDI1_TXN[2]
DDI1_TXP[2]
DDI1_TXN[3]
DDI1_TXP[3]

DDI

EDP

EDP_TXN[0]
EDP_TXP[0]
EDP_TXN[1]
EDP_TXP[1]
EDP_TXN[2]
EDP_TXP[2]
EDP_TXN[3]
EDP_TXP[3]

C47 INT_EDP_TXN0
C46 INT_EDP_TXP0
C45 INT_EDP_TXN1
C45 INT_EDP_TXP1
C45 INT_EDP_TXN2
C45 INT_EDP_TXP2
C47 INT_EDP_TXN3
C47 INT_EDP_TXP3

INT_EDP_TXN0 [25]
INT_EDP_TXP0 [25]
INT_EDP_TXN1 [25]
INT_EDP_TXP1 [25]
INT_EDP_TXN2 [25]
INT_EDP_TXP2 [25]
INT_EDP_TXN3 [25]
INT_EDP_TXP3 [25]

EDP_AUXN
EDP_AUXP
EDP_DISP_UTIL
DDI1_AUXN
DDI1_AUXP
DDI2_AUXN
DDI2_AUXP
DDI3_AUXN
DDI3_AUXP

F45 INT_EDP_AUXN
F45 INT_EDP_AUXP
B52 EDP_DISP_UTIL
G50
F50
C48
C46
C46
L9
L7
L6
L9
L10

INT_EDP_AUXN [25]
INT_EDP_AUXP [25]
TP1
HDMI_HPD_CON [27]
ULT_EDP_HPD [25]
PCH_LVDS_BLON [25]
PCH_DPST_PWM [25]
PCH_DISP_ON [25]

[27] SDVO_CLK
[27] SDVO_DATA

TP2

DDPC_CTRLDATA

TP3

DDPC_CTRLDATA

+VCCIO
R3 24.9/F 4 EDP_RCOMP

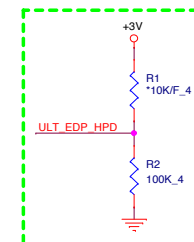
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

*SKL_ULT
REV = 1

1 OF 20

?

Reserve EDP_HPD opposites circuit!



+VCCSTPLL
R6 49.9/F 4 CATERR#

+1.0V
R9 0.4

R10 51.4 JTAGX_PCH
R13 51.4 JTAG_TMS_PCH
R15 51.4 JTAG_TDI_PCH
R16 51.4 JTAG_TDO_PCH
R18 51.4 JTAG_TCK_PCH

Close to Chipset

[33,39,47] H_PROCHOT#
R4 49.9/F 4 EC_PECI
[33] PM_THRMTRIP#

CATERR#
EC_PECI
PROCHOT#
PM_THRMTRIP#

U1D

SKL_ULT ?

Need apply PN

De3 CATERR#
A51 EC_PECI
C55 PROCHOT#
A61 PM_THRMTRIP#
C55 BPM#0
B54 BPM#1
C55 BPM#2
C55 BPM#3

PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#

B61 XDP_TCK0
B60 XDP_TDI_CPU
A61 XDP_TDO_CPU
C60 XDP_TMS_CPU
B59 XDP_TRST#_CPU

XDP_TCK0 [16]
XDP_TDI_CPU [16]
XDP_TDO_CPU [16]
XDP_TMS_CPU [16]
XDP_TRST#_CPU [2,16]

3D_FW_GPIO_R
CPU_GP1
CPU_GP2
CPU_GP3

A6
A7
BA5
AY5

PROC_POPIRCOMP
PROC_OPIRCOMP
PROC_OPCIRCOMP
PROC_OPC_RCOMP
PROC_OPC_RCOMP

B56 JTAG_TCK_PCH
D59 JTAG_TDI_PCH
A56 JTAG_TDO_PCH
C59 JTAG_TMS_PCH
C61 XDP_TRST#_CPU
A59 JTAGX_PCH

JTAG_TCK_PCH [16]
JTAG_TDI_PCH [16]
JTAG_TDO_PCH [16]
JTAG_TMS_PCH [16]
XDP_TRST#_CPU [2,16]
JTAGX_PCH [16]

PROC_POPIRCOMP
PROC_OPIRCOMP
PROC_OPCIRCOMP
PROC_OPC_RCOMP
PROC_OPC_RCOMP

AT16
AU16
H66
H65

PROC_POPIRCOMP
PROC_OPIRCOMP
PROC_OPCIRCOMP
PROC_OPC_RCOMP
PROC_OPC_RCOMP

PROC_POPIRCOMP
PROC_OPIRCOMP
PROC_OPCIRCOMP
PROC_OPC_RCOMP
PROC_OPC_RCOMP

PROC_POPIRCOMP
PROC_OPIRCOMP
PROC_OPCIRCOMP
PROC_OPC_RCOMP
PROC_OPC_RCOMP

*SKL_ULT

REV = 1

4 OF 20

Close to EC

PM_THRMTRIP# R5 1K 4
+VCCSTPLL
Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL
470 OHM IS FOR I/P

PLACE NEAR CPU

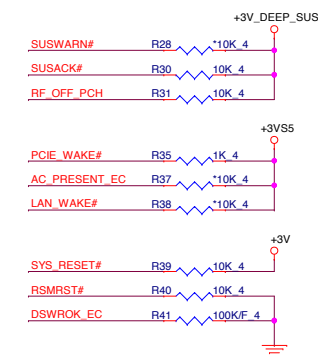
XDP_TMS_CPU R17 51.4
XDP_TDI_CPU R19 51.4
XDP_TDO_CPU R20 51.4
+1.0V

H_PROCHOT# R21 1K 4
XDP_TCK0 R22 51.4
XDP_TRST#_CPU R23 51.4
+1.0V



PROJECT : G34A
Quanta Computer Inc.

Size Custom	Document Number 02 - SKYPAKE 1/20(eDP/DDI)	Rev 1A
Date: Tuesday, January 05, 2016	Sheet 2 of 47	

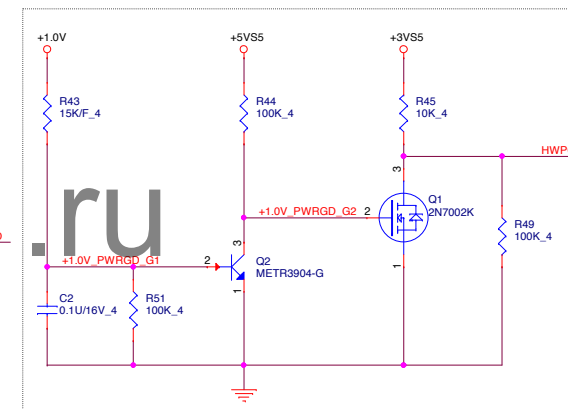
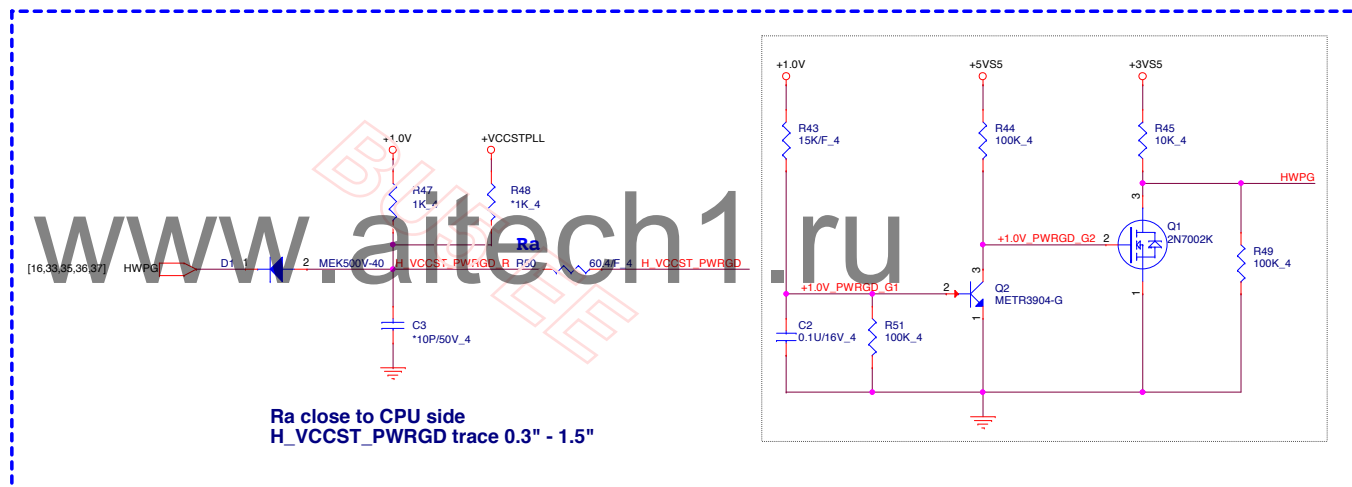


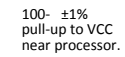
For DS3 -->Ra
Non-DS3 -->Rb

RSMRST# R42 Rb *0.4

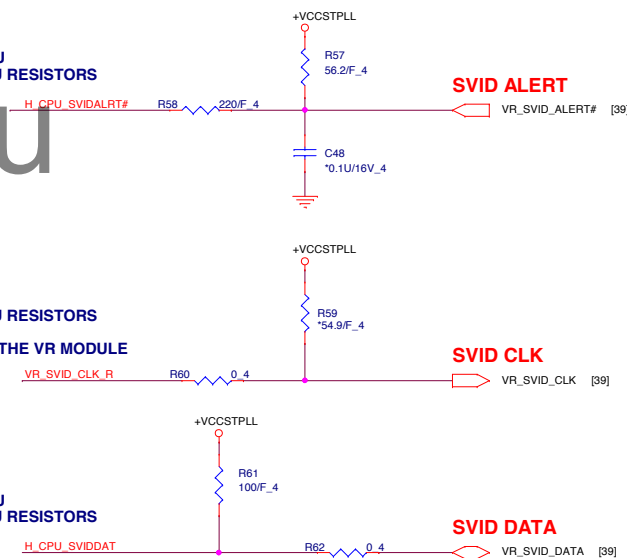
EC R46 Ra 0.4 DSWROK_EC_R

Check Rise/Fall time less than 100ns






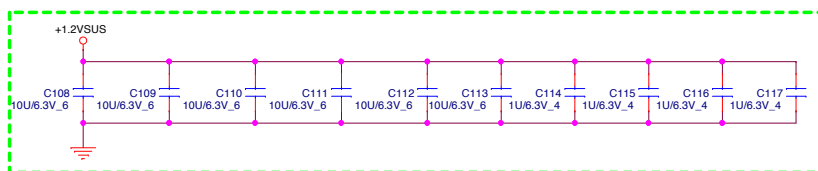
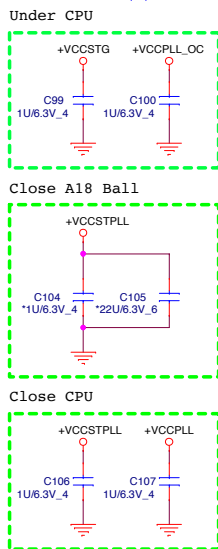
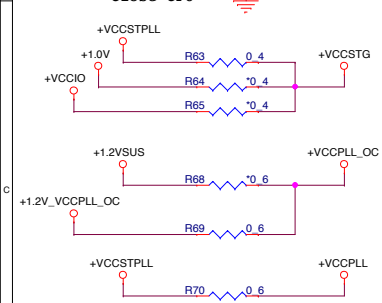
**CLOSE TO CPU
PLACE THE PU RESISTORS**



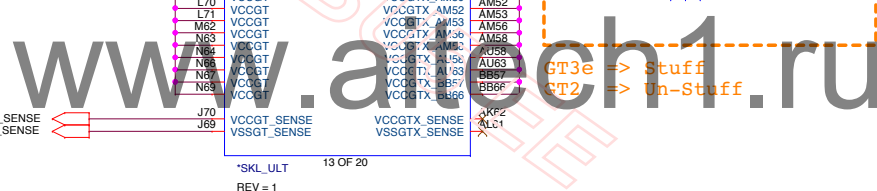
**PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE**


**CLOSE TO CPU
PLACE THE PU RESISTORS**

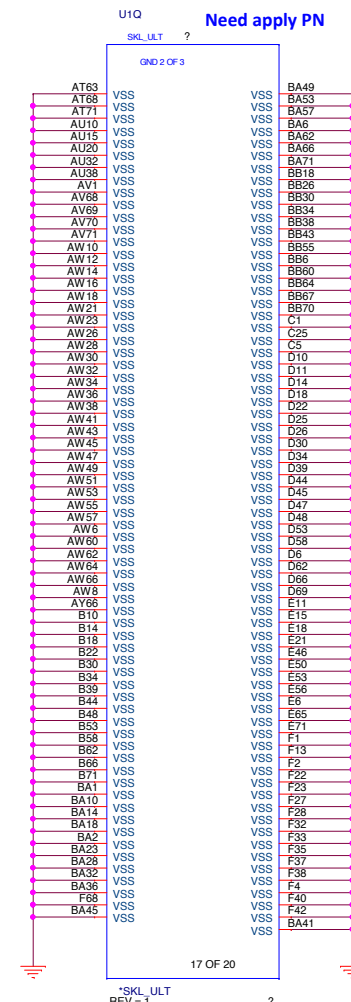
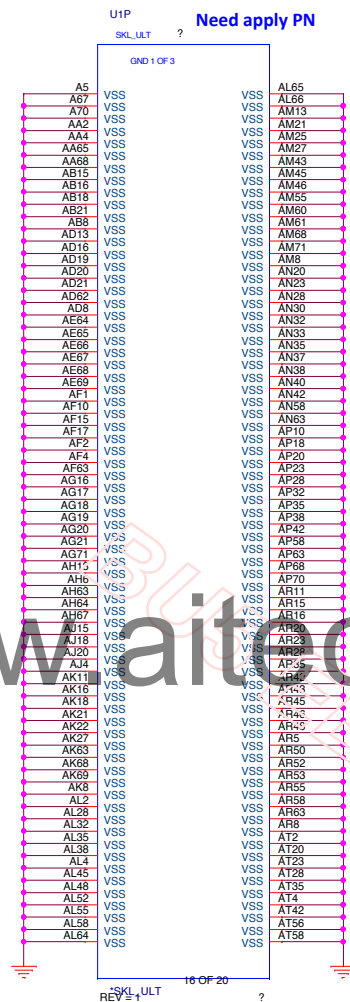
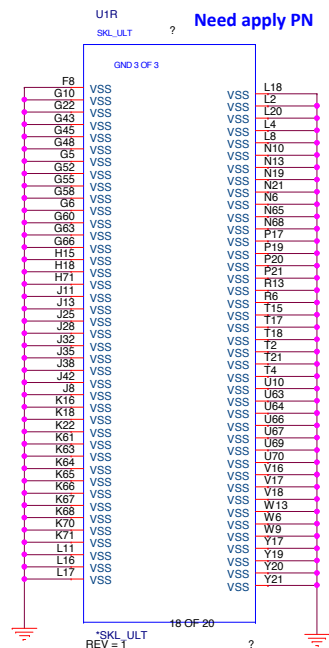
 BU5	PROJECT : G34A Quanta Computer Inc.		
	Size Custom	Document Number 05 -- SKYPAKE 6/20 (POWER-1)	Rev 1A
	Date: Tuesday, January 05, 2016	Sheet	5 of 47

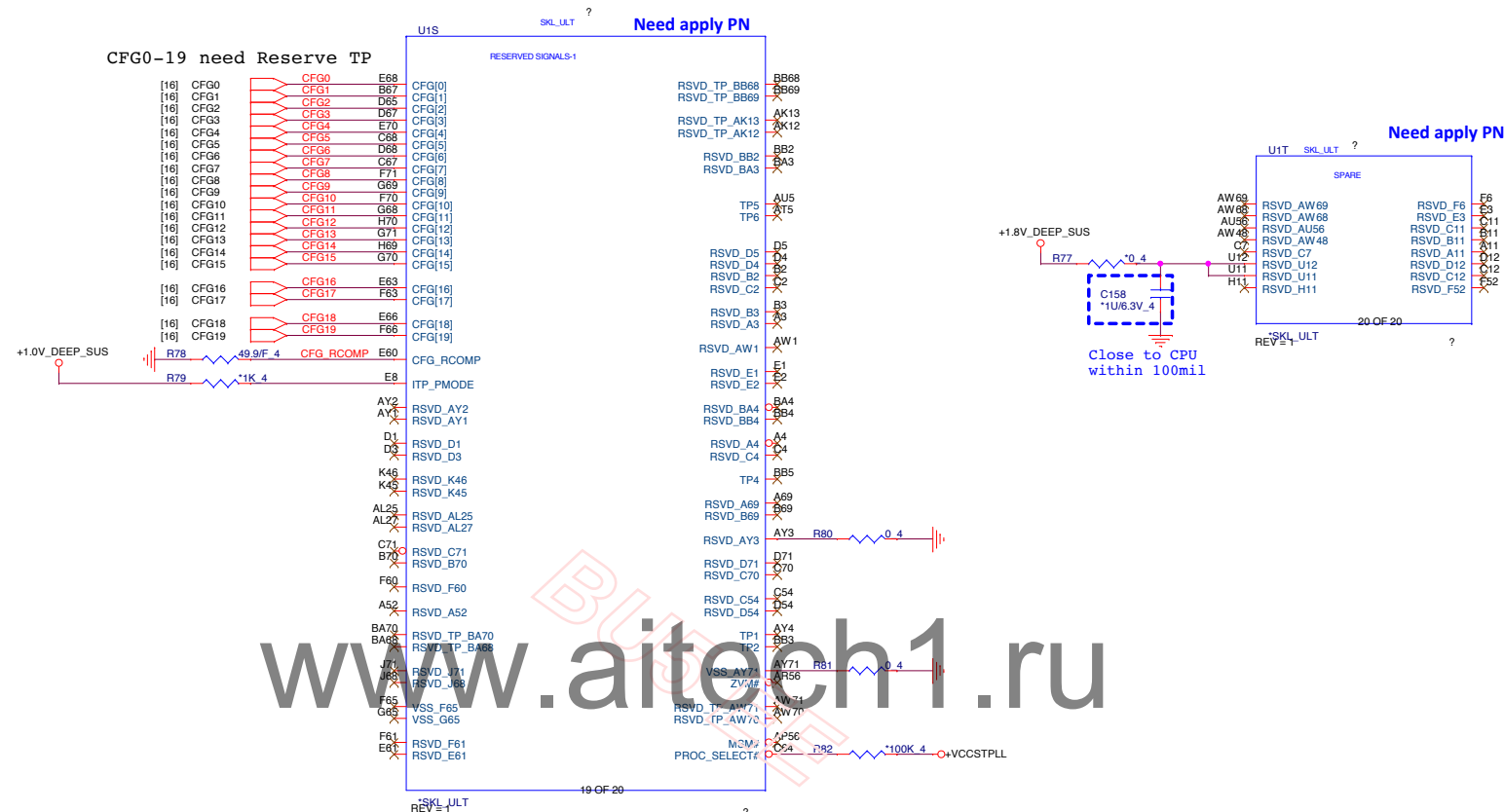


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



	PROJECT : G34A Quanta Computer Inc.		
	Size Custom	Document Number 07 -- SKYPAKE 8/20 (POWER-3)	Rev 1A
	Date: Tuesday, January 05, 2016	Sheet 7 of 47	











Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K 4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 *1K 4



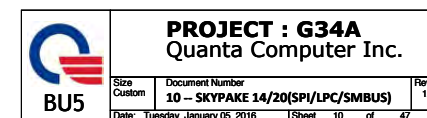
[33]	PCH_SPI_CS0#_R	PCH_SPI_CS0#_R
[33]	PCH_SPI1_CLK_R	PCH_SPI1_CLK_R
[33]	PCH_SPI1_SI_R	PCH_SPI1_SI_R
[33]	PCH_SPI1_SO_R	PCH_SPI1_SO_R

TP17		PCH SPI CS0# R
TP18		PCH SPI1 CLK R
TP19		PCH SPI1 SI R
TP20		PCH SPI1 SO R
TP21		BIOS WP#
TP22		HOLD#

PCH SPI ROM(CLG)

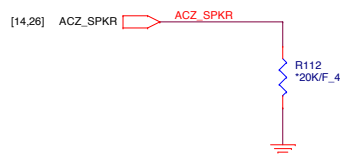


SMBus/Pull-up(CLG)

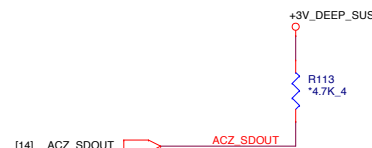


Functional Strap Definitions

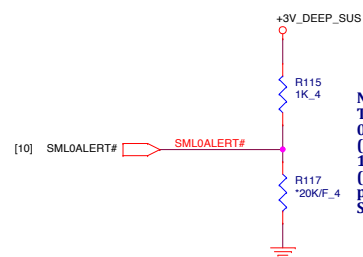
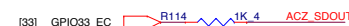
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



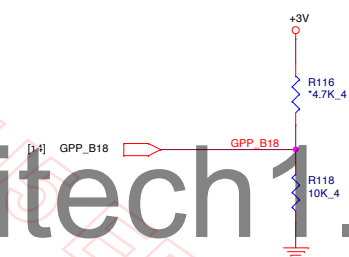
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



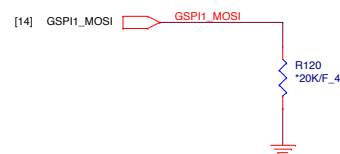
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



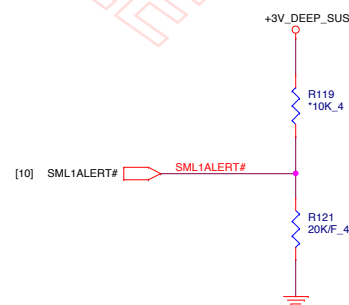
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC



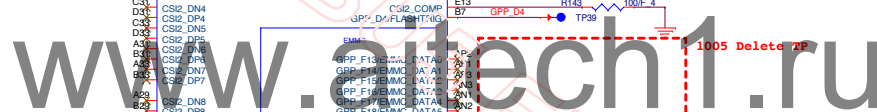
No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

Need apply PN

SSIC / USB3

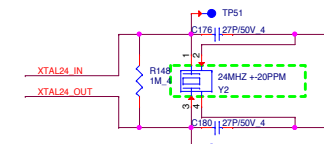
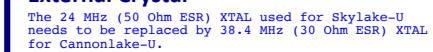
USB3_2_RXN/SSIC_2_RXN
USB3_2_RXP/SSIC_2_RXP
USB3_2_TXN/SSIC_2_TXN
USB3_2_TXP/SSIC_2_TXPUSB3_3_RXN/SSIC_3_RXN
USB3_3_RXP/SSIC_3_RXP
USB3_3_TXN/SSIC_3_TXN
USB3_3_TXP/SSIC_3_TXPUSB2N_1
USB2P_1USB2N_2
USB2P_2USB2N_3
USB2P_3USB2N_4
USB2P_4USB2N_5
USB2P_5USB2N_6
USB2P_6USB2N_7
USB2P_7USB2N_8
USB2P_8USB2N_9
USB2P_9USB2N_10
USB2P_10USB2N_11
USB2P_11USB2N_12
USB2P_12USB2N_13
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USB2P_216USB2N_217
USB2P_217USB2N_218
USB2P_218USB2N_219
USB2P_219USB2N_220
USB2P_220USB2N_221
USB2P_221USB2N_222
USB2P_222USB2N_223
USB2P_223USB2N_224
USB2P_224USB2N_225
USB2P_225USB2N_226
USB2P_226USB2N_227
USB2P_227USB2N_228
USB2P_228USB2N_229
USB2P_229USB2N_230
USB2P_230USB2N_231
USB2P_231USB2N_232
USB2P_232USB2N_233
USB2P_233USB2N_234
USB2P_234USB2N_235
USB2P_235USB2N_236
USB2P_236USB2N_237
USB2P_237USB2N_238
USB2P_238USB2N_239
USB2P_239USB2N_240
USB2P_240USB2N_241
USB2P_241USB2N_242
USB2P_242USB2N_243
USB2P_243USB2N_244
USB2P_244USB2N_245
USB2P_245USB2N_246
USB2P_246USB2N_247
USB2P_247USB2N_248
USB2P_248USB2N_249
USB2P_249USB2N_250
USB2P_250USB2N_251
USB2P_251USB2N_252
USB2P_252USB2N_253
USB2P_253USB2N_254
USB2P_254USB2N_255
USB2P_255USB2N_256
USB2P_256USB2N_257
USB2P_257

USB

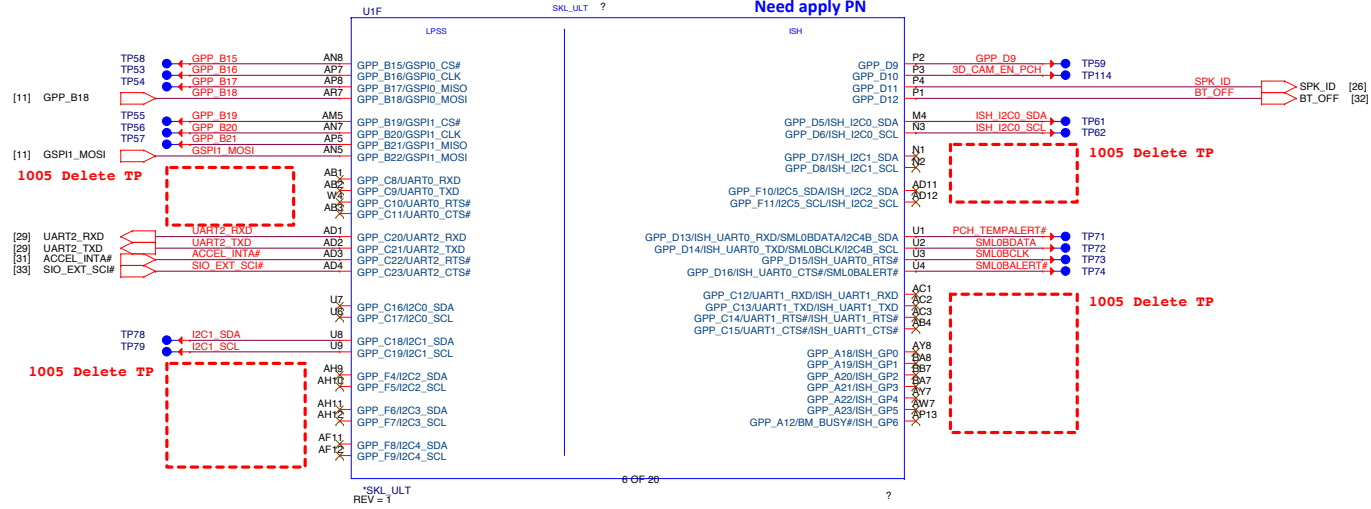
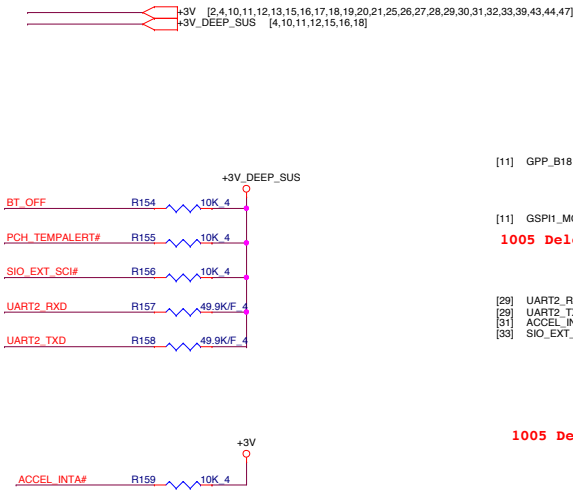


30mils

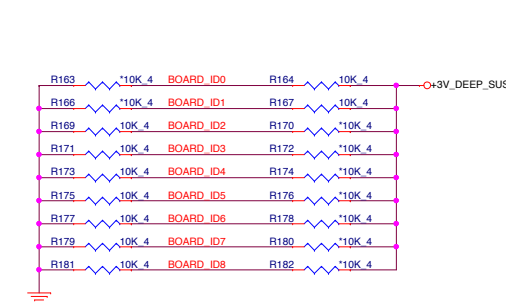
TC 2 +BAT RTC 1005 Change +3V_RTC to +BAT RTC



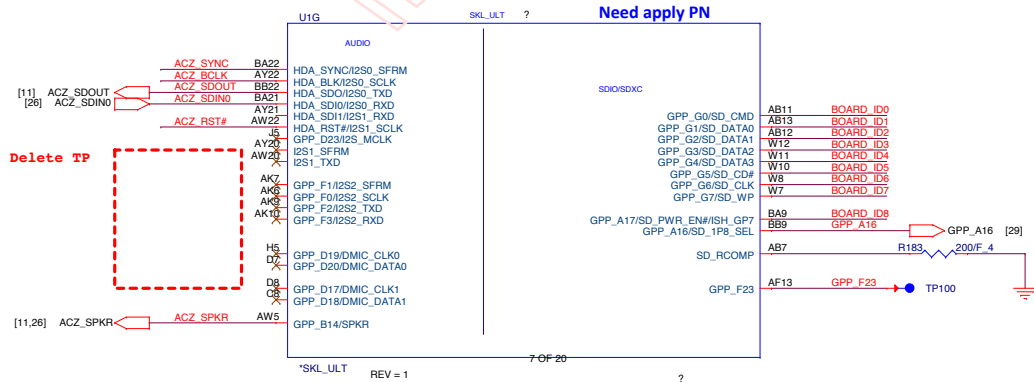
Skylake (GPIO)

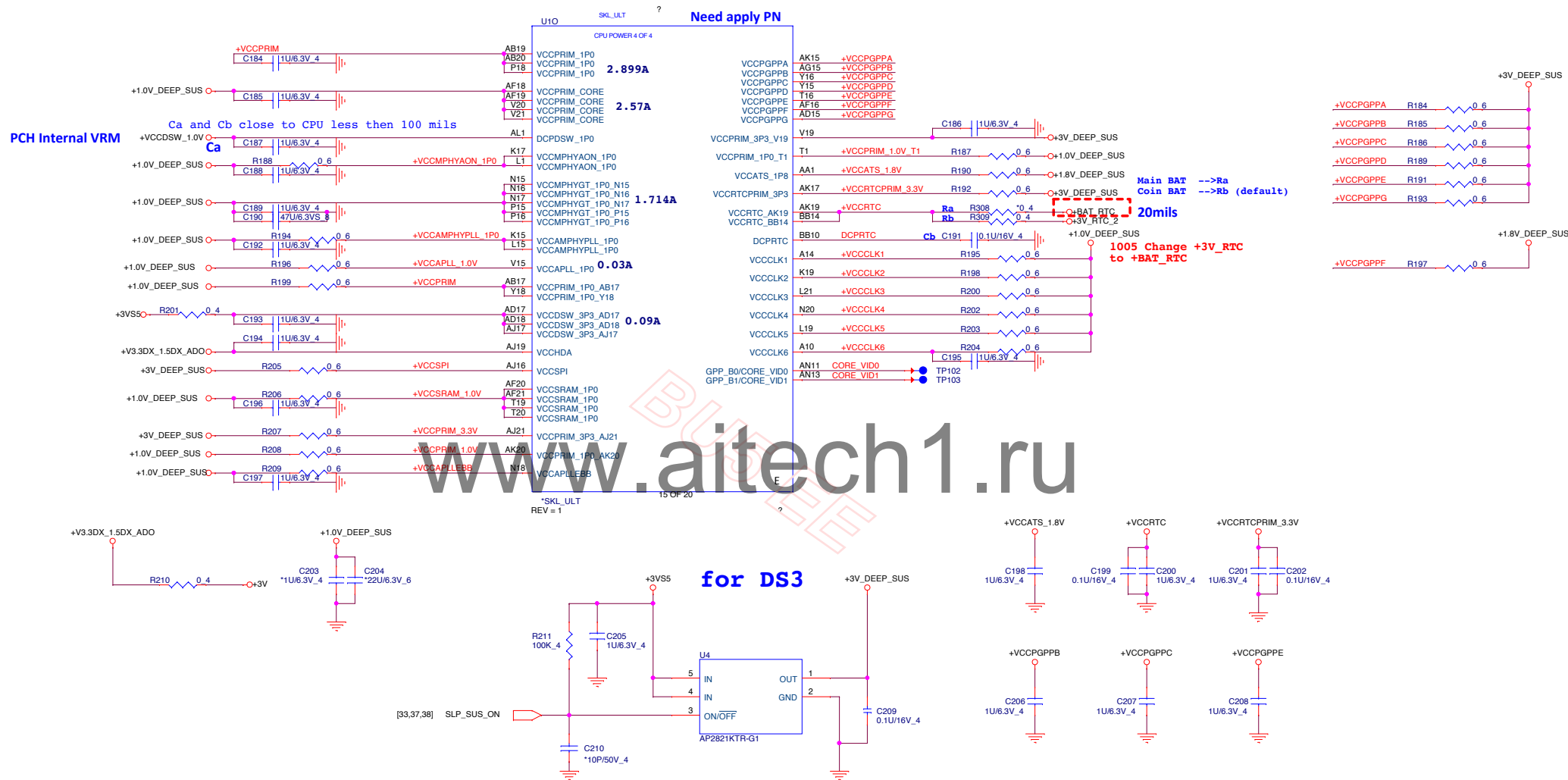


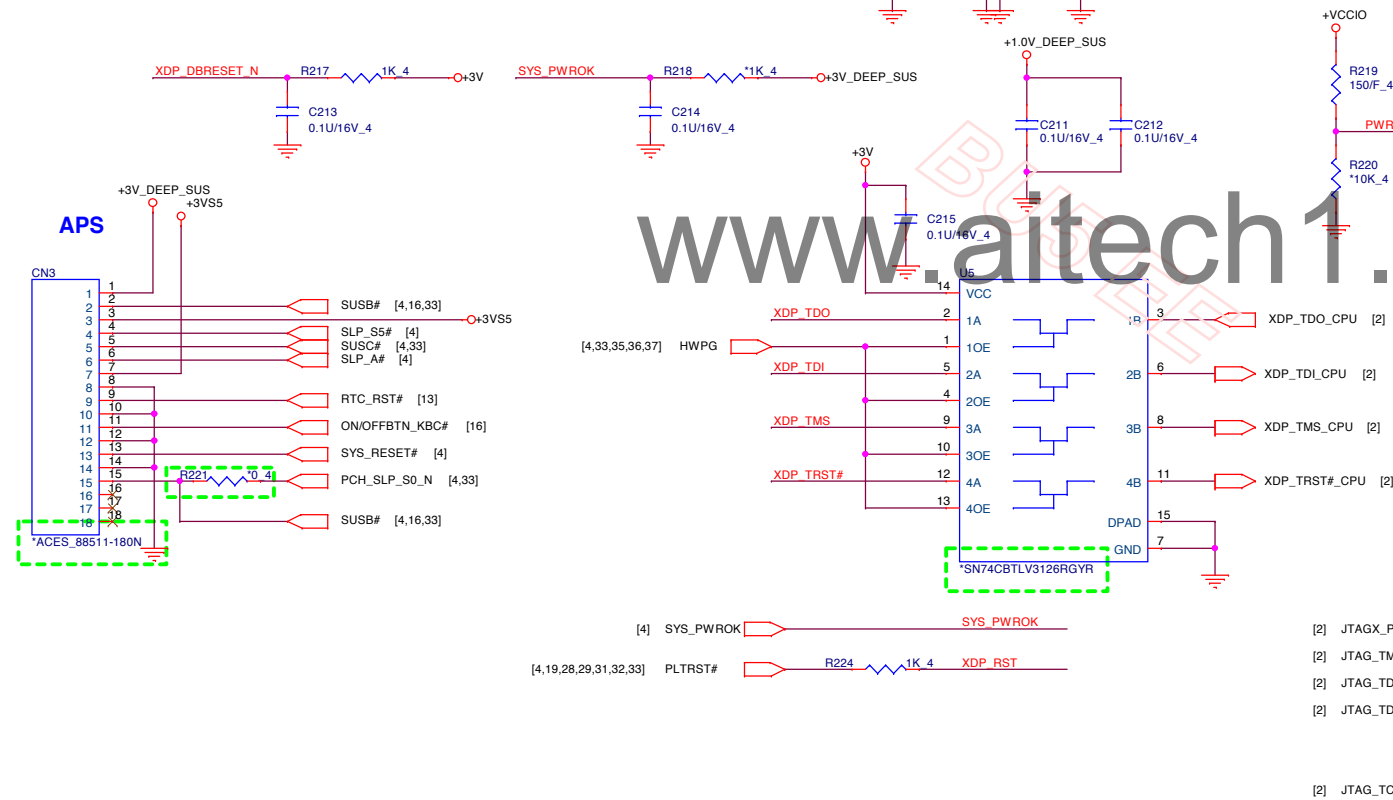
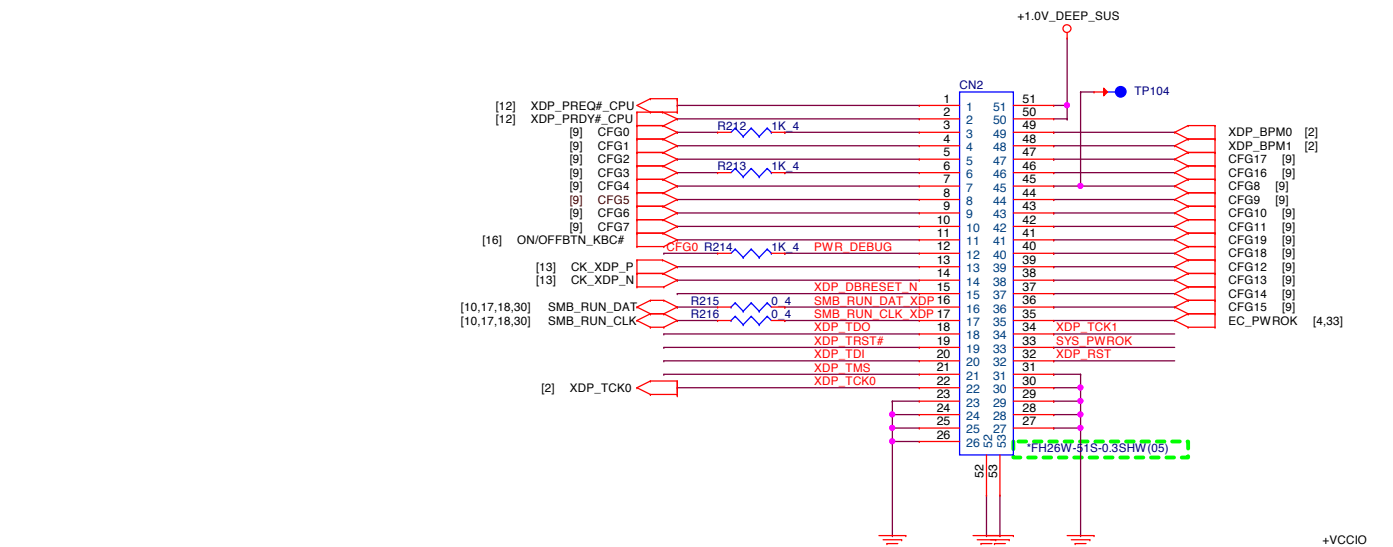
HDA Bus(CLG)



Skylake	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	Reserve (Default = 00)	00 14" 01 15" 10 Reserve 11 Reserve	0 : UMA 1 : DIS

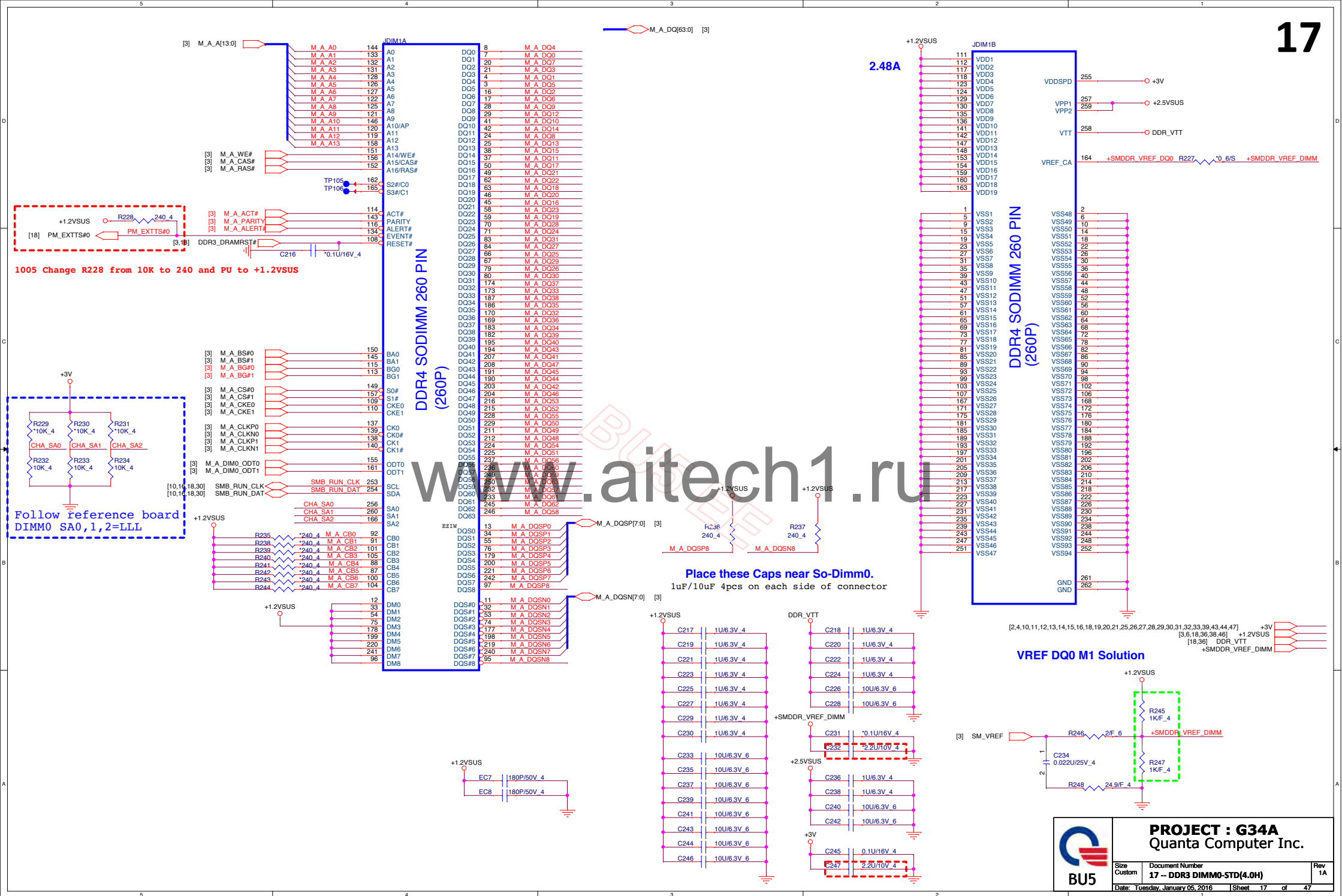




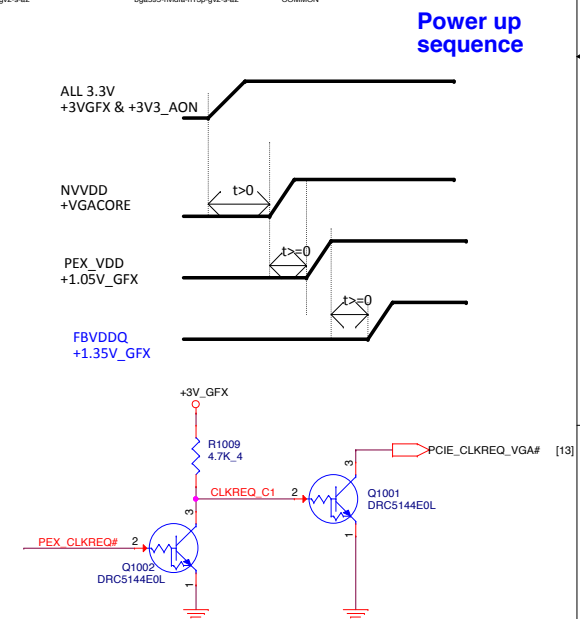
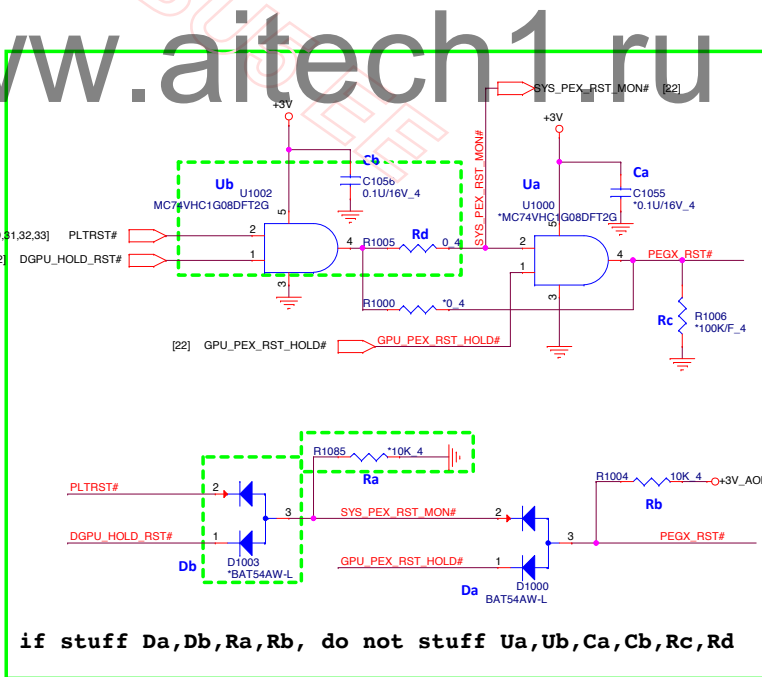
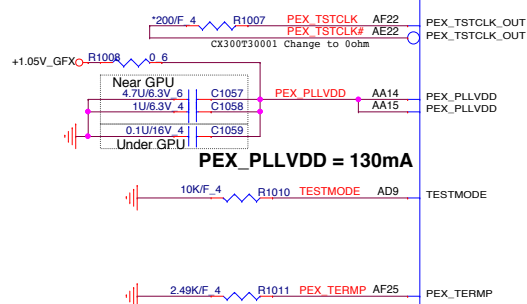
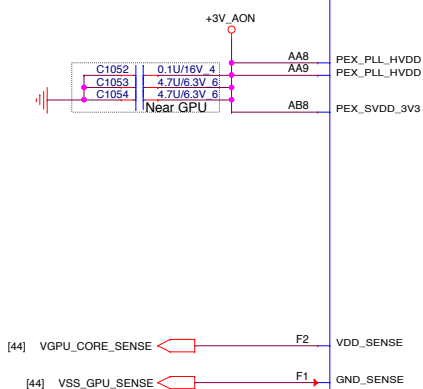
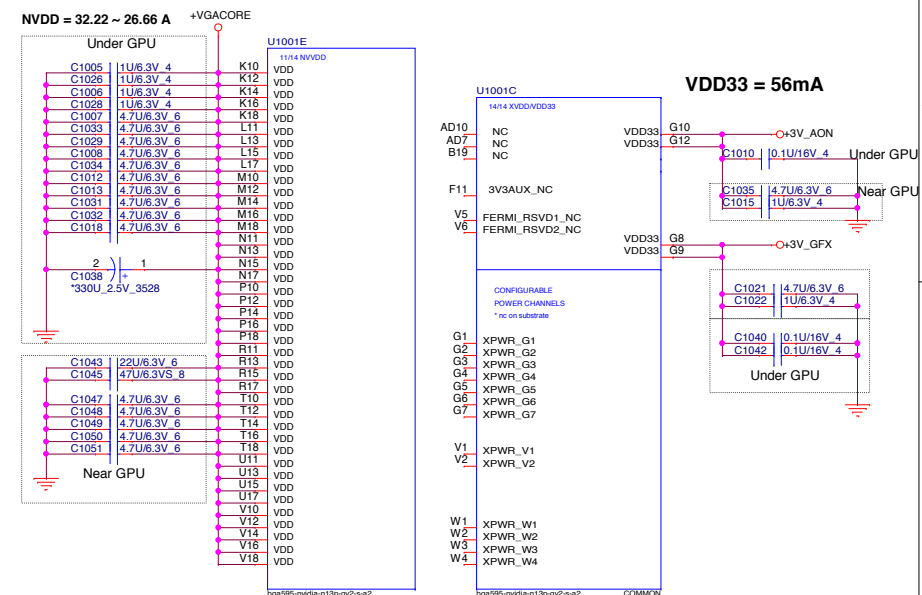
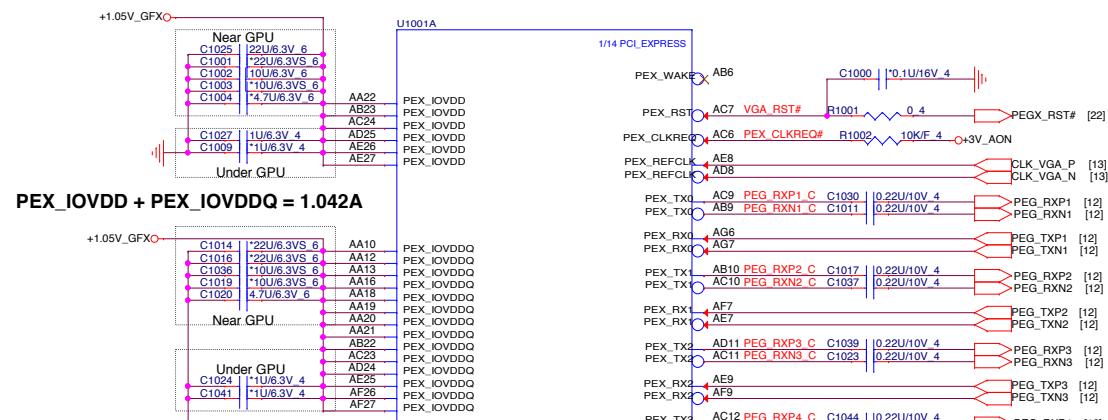


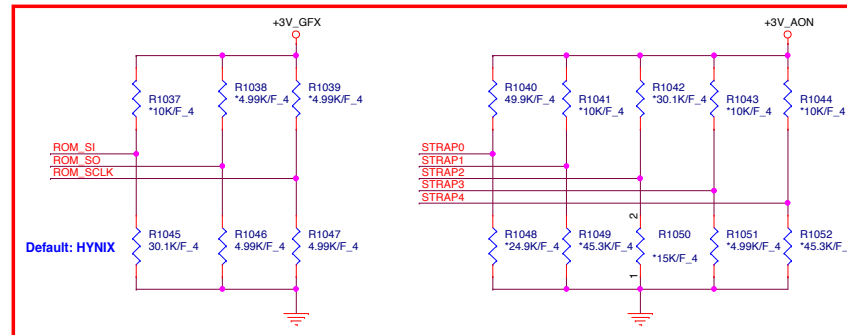
PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
	16 -- HSW XDP & APS	1A
Date: Tuesday, January 05, 2016	Sheet 16 of 47	

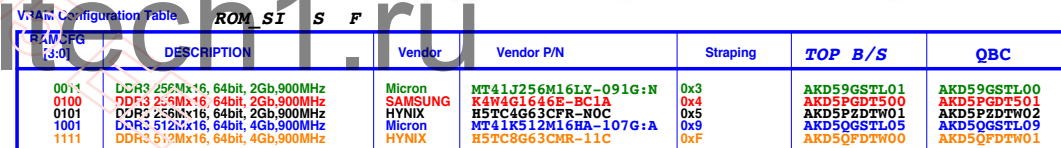




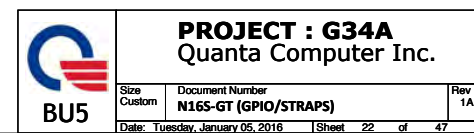
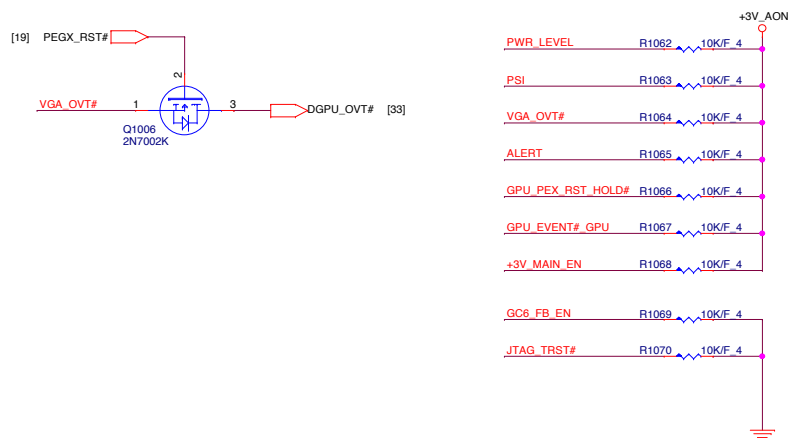




Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

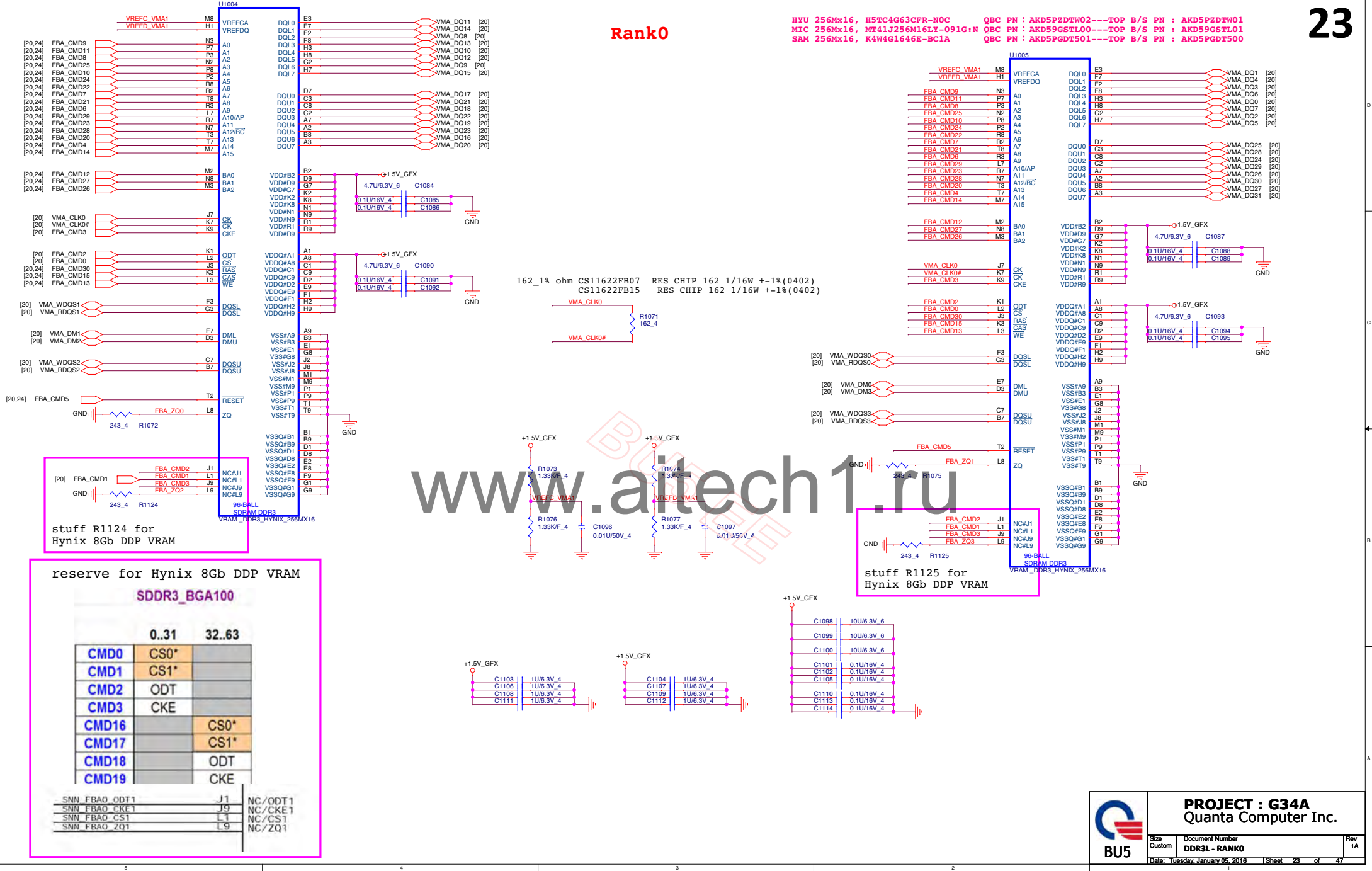


GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



Rank0

HYU 256Mx16, H5TC4G63CFR-NOC QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16LY-091G:N QBC PN : AKD59GSTL00---TOP B/S PN : AKD59GSTL01
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500



stuff R1124 for
Hynix 8Gb DDP VRAM

reserve for Hynix 8Gb DDP VRAM

SDDR3_BGA100

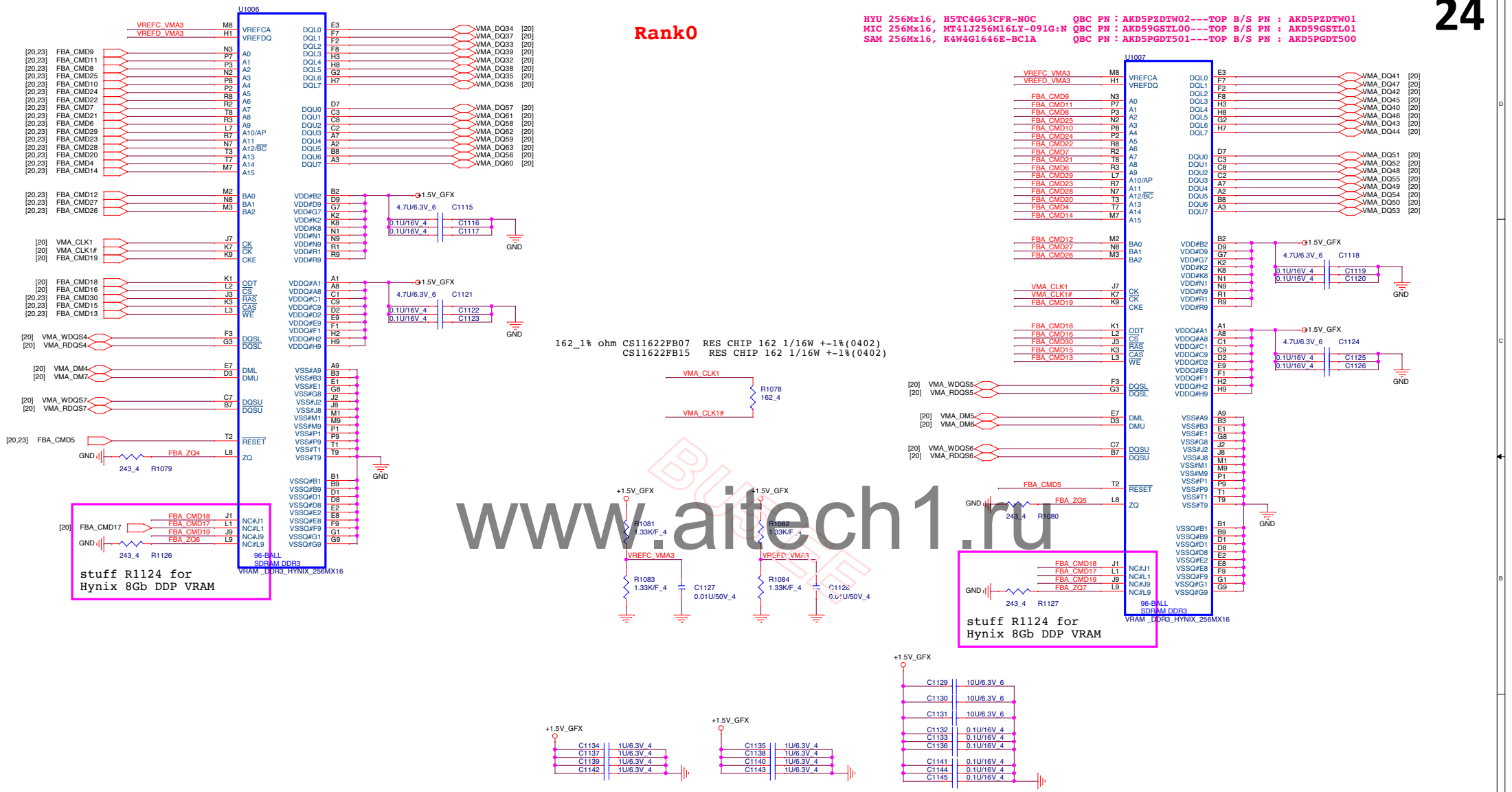
	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN FBAO ODT1	J1	NC/ODT1
SNN FBAO CKE1	J9	NC/CKE1
SNN FBAO CS1	L1	NC/CS1
SNN FBAO ZQ1	L9	NC/ZQ1

stuff R1125 for
Hynix 8Gb DDP VRAM

Rank0

HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, M141J256M16LY-091G:N QBC PN : AKD59GSTL00---TOP B/S PN : AKD59GSTL01
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500

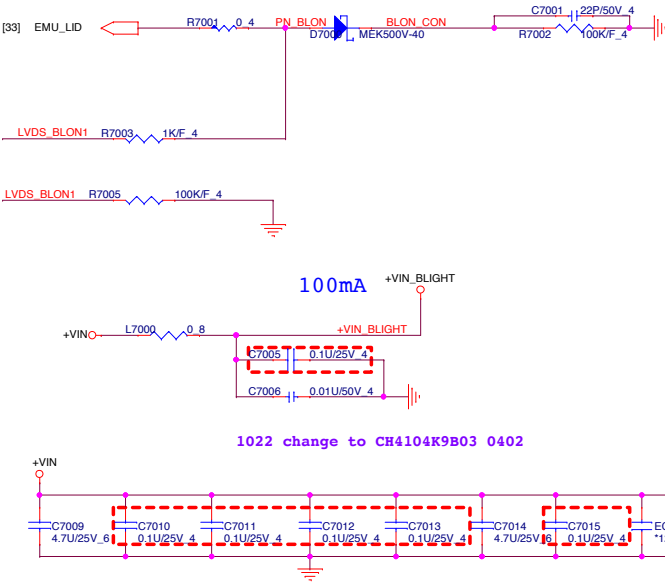


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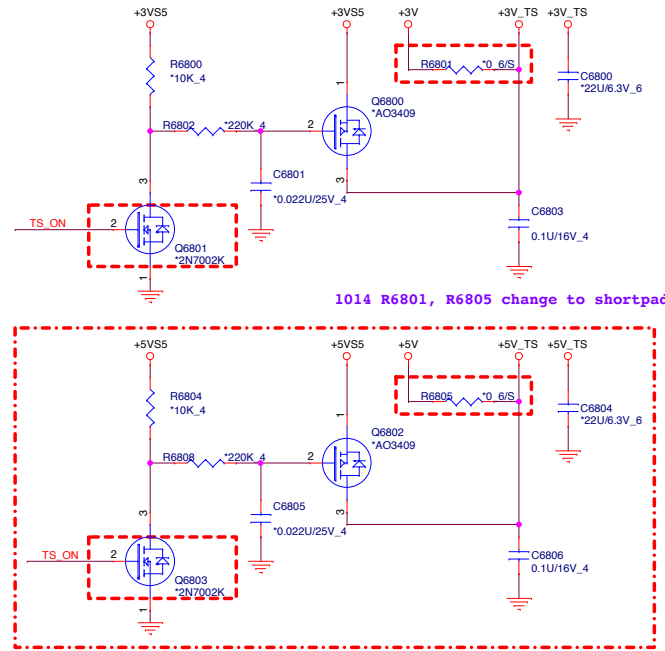
stuff R1124 for
Hynix 8Gb DDP VRAM

stuff R1124 for
Hynix 8Gb DDP VRAM

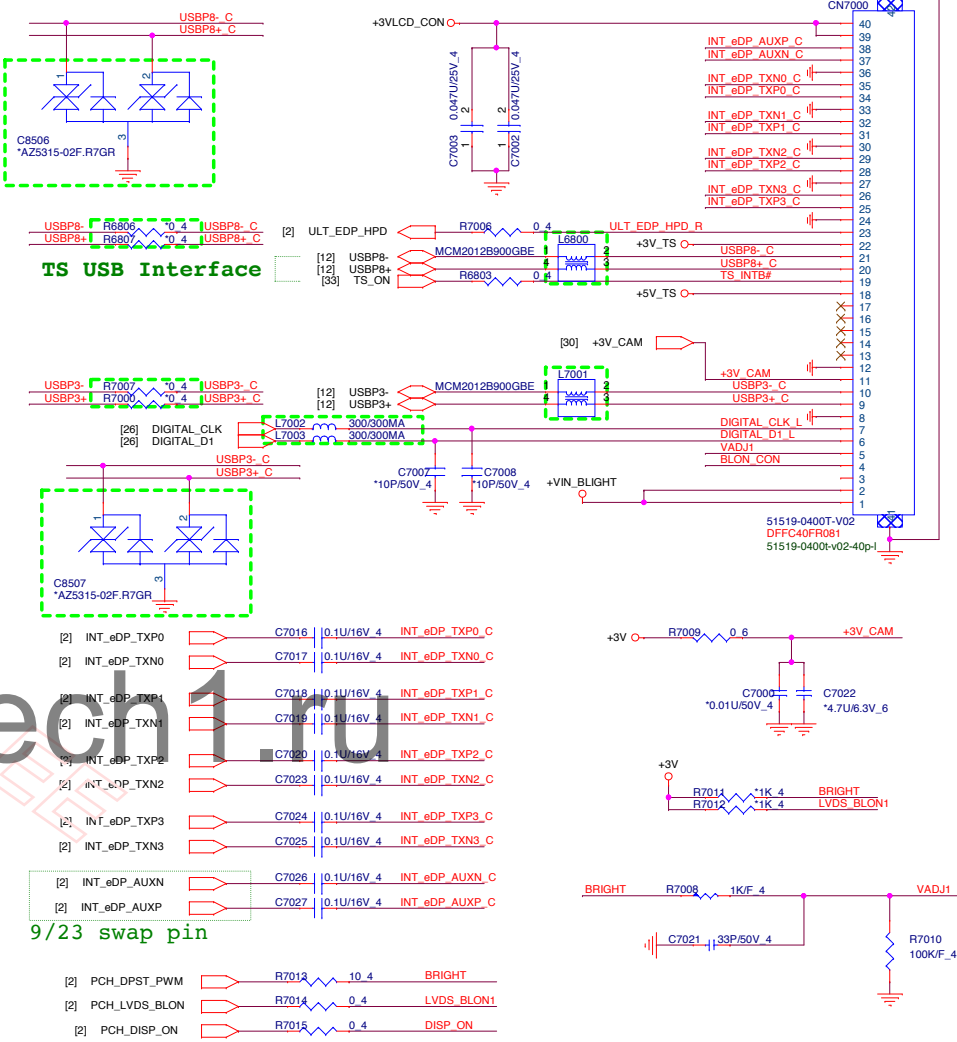
LID Switch



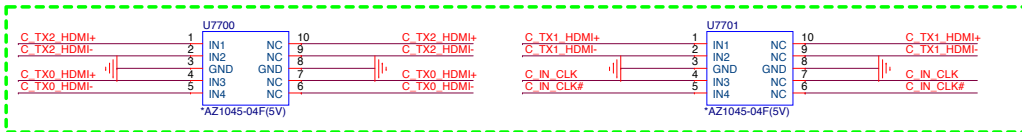
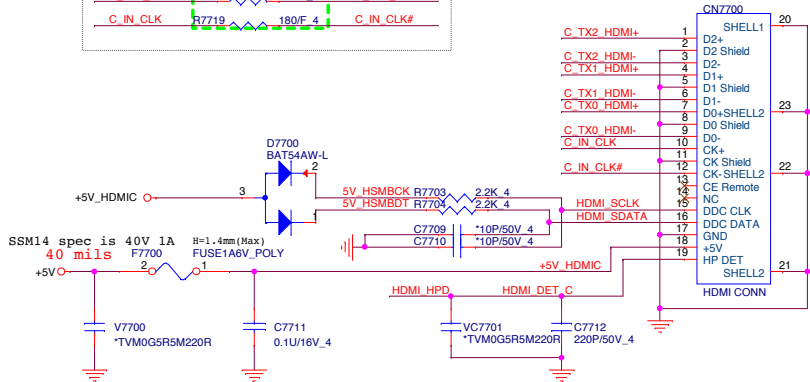
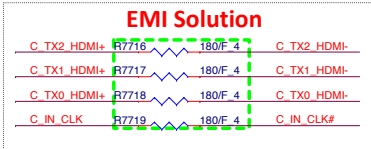
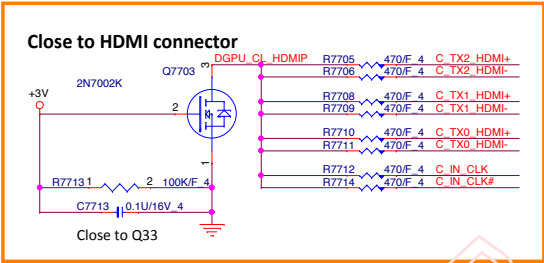
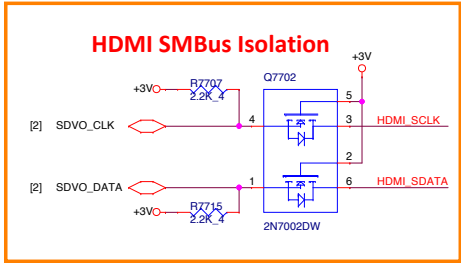
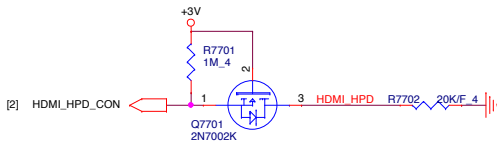
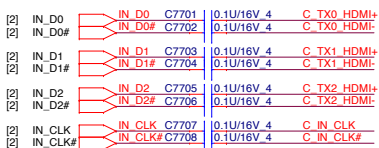
Touch screen



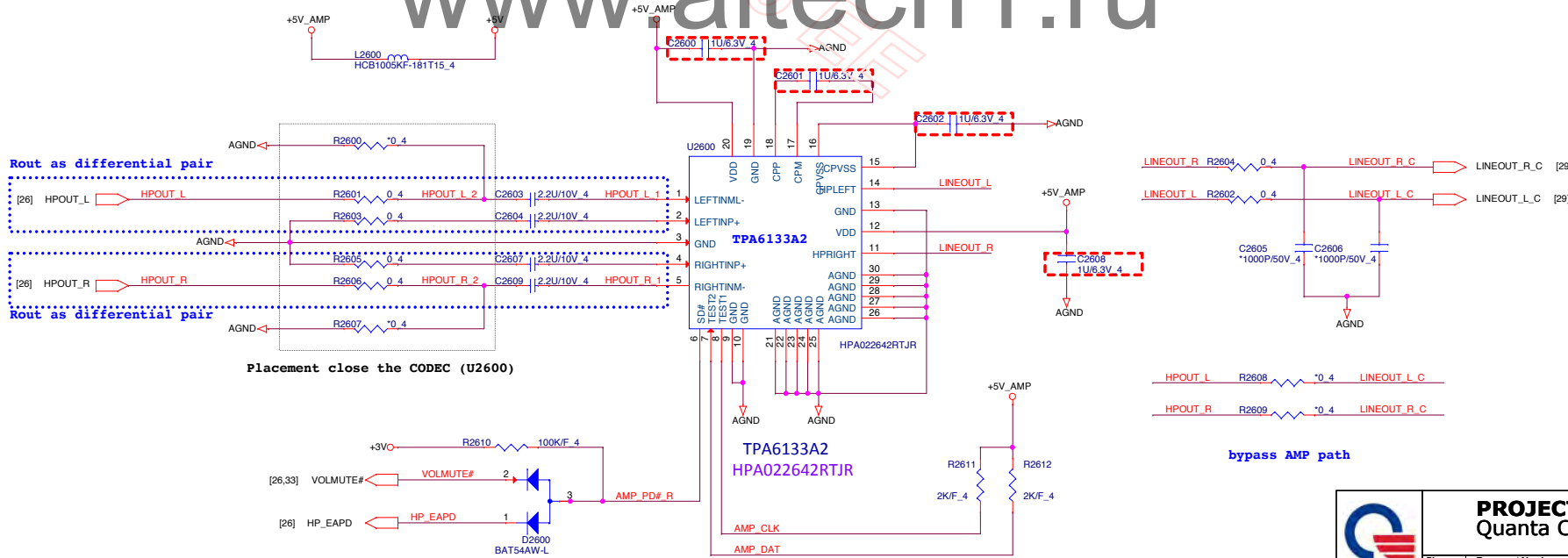
eDP Conn.



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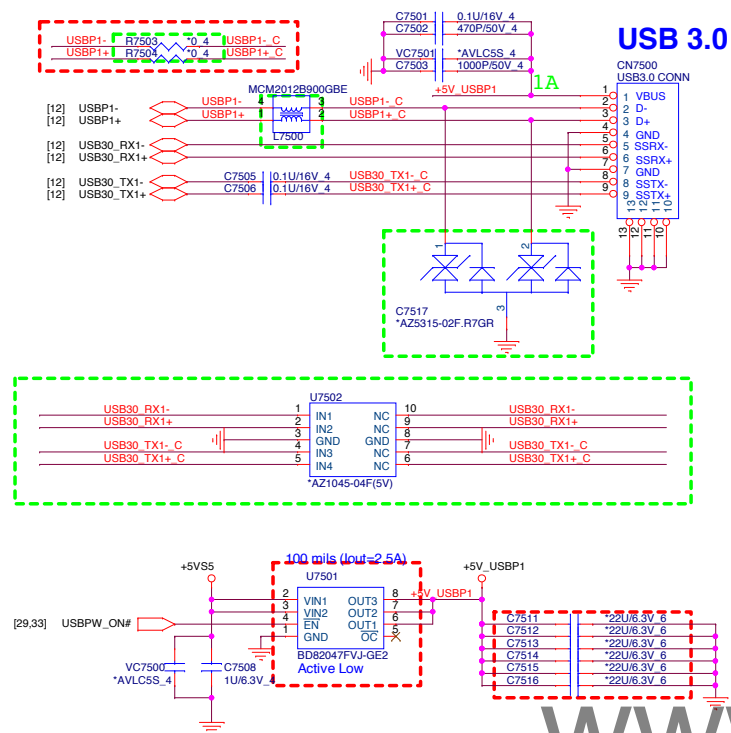


Head Phone out

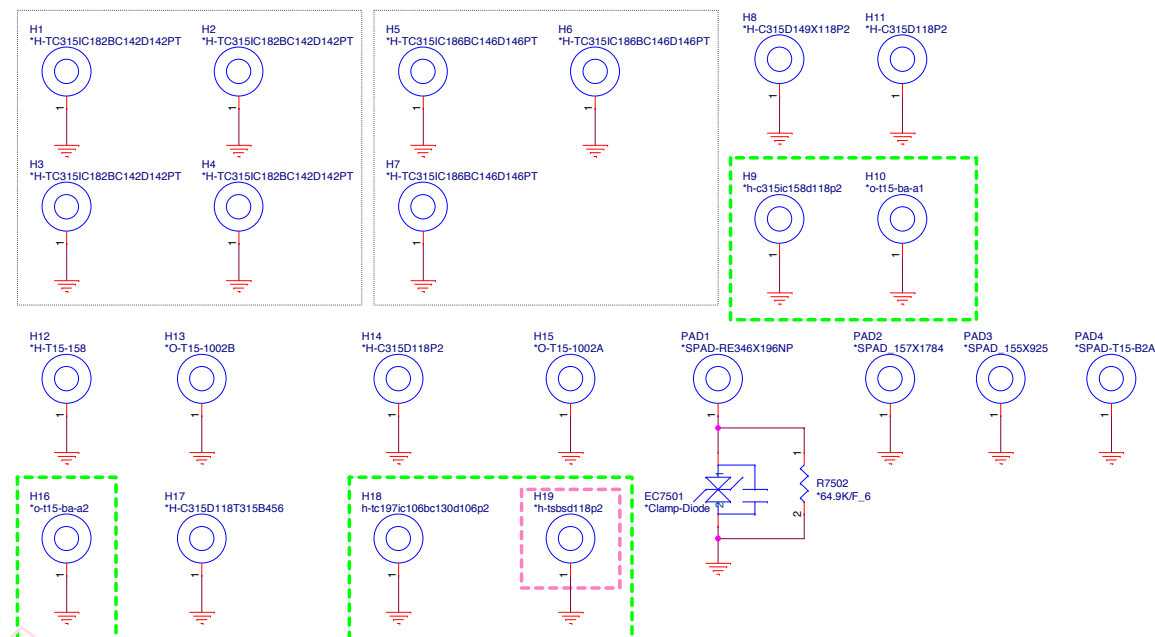




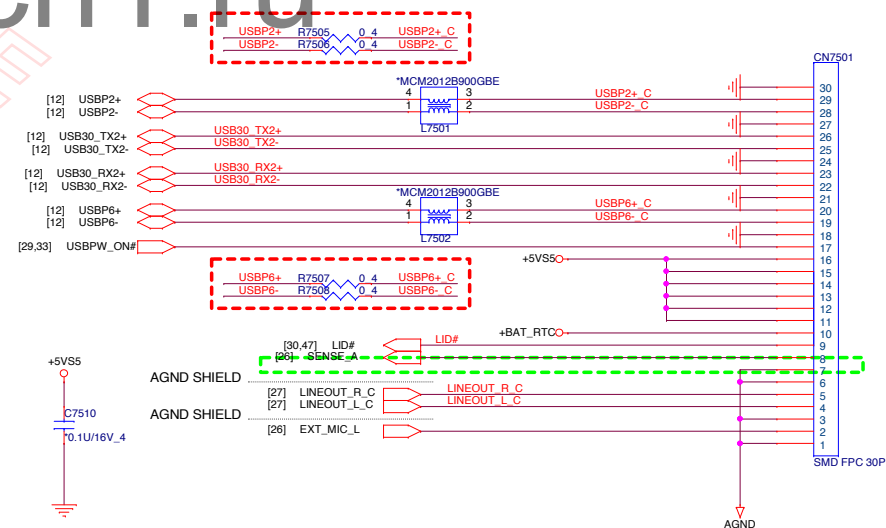
USB 2.0/3.0 Combo



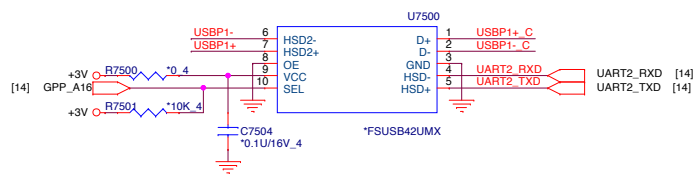
Holes



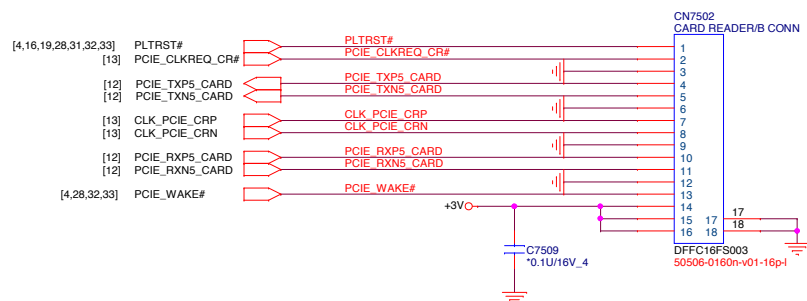
USB/Phone Jack Connector



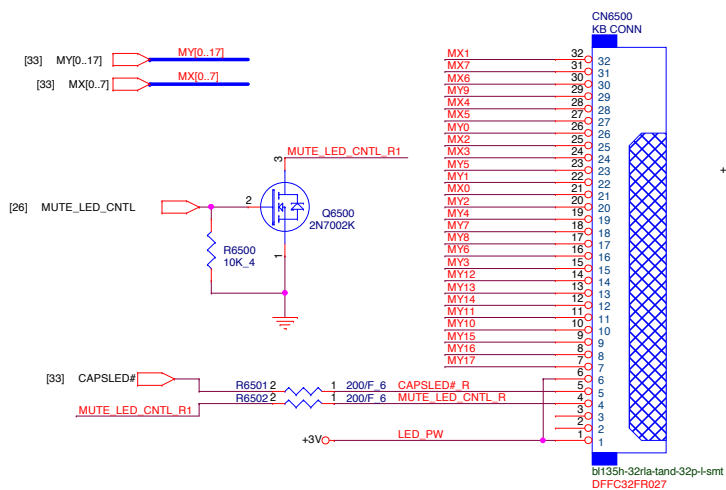
UART for DEBUG



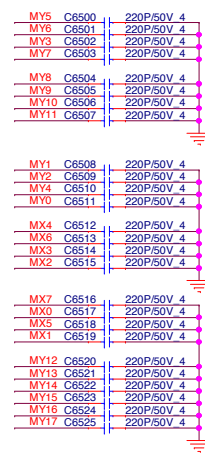
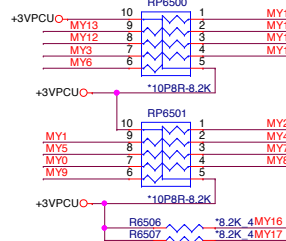
Card Reader Connector



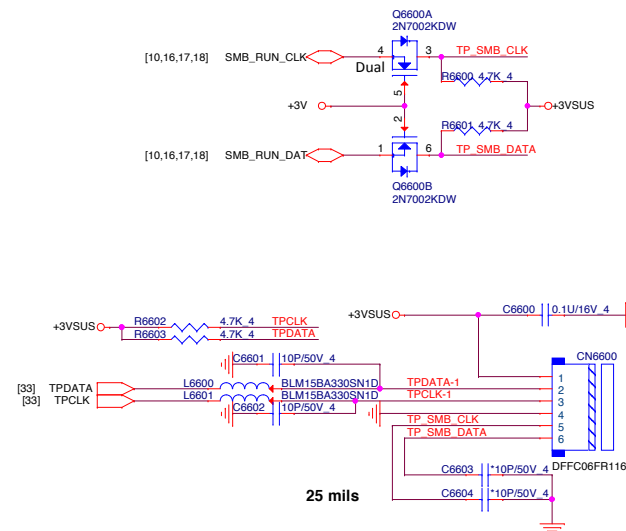
KEYBOARD Con.



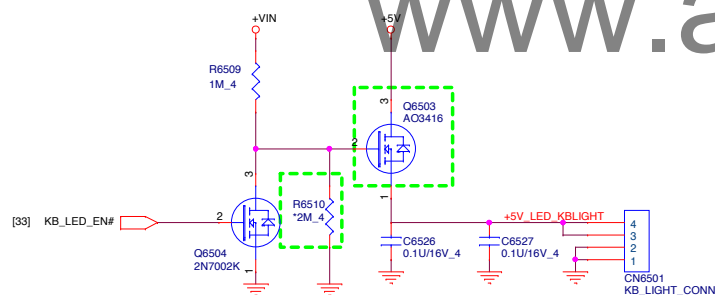
KEYBOARD PULL-UP



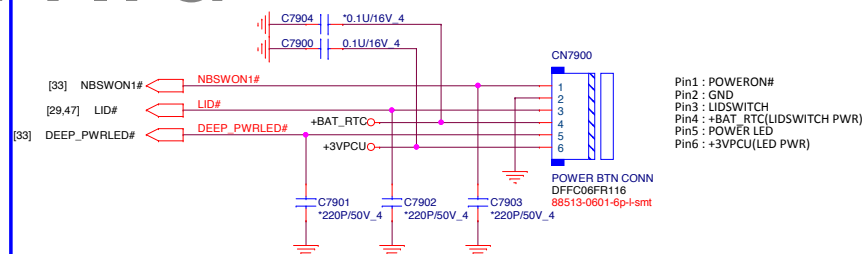
Touch Pad Connector



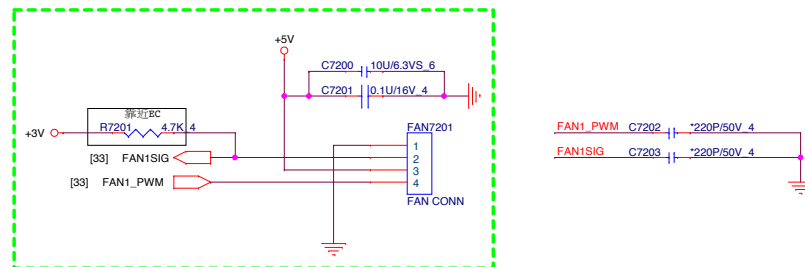
KB LIGHT CONN



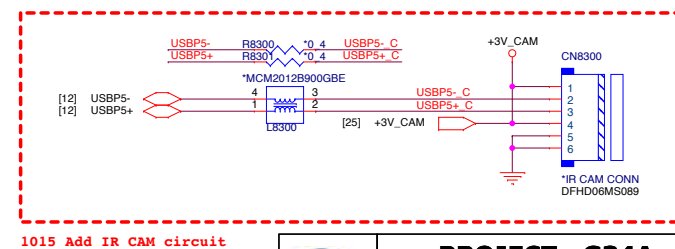
Power Button Connector



FAN CONN

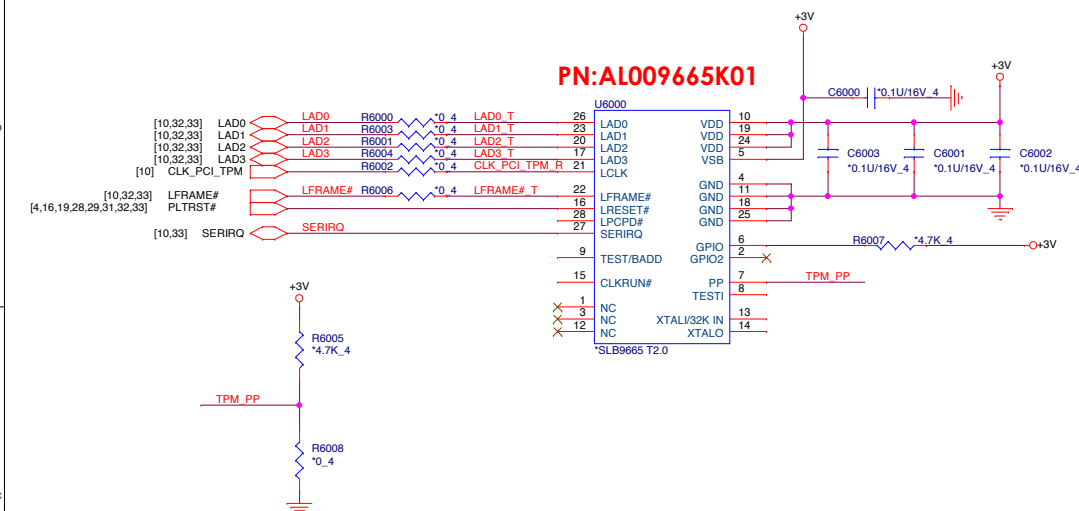


IR CAM

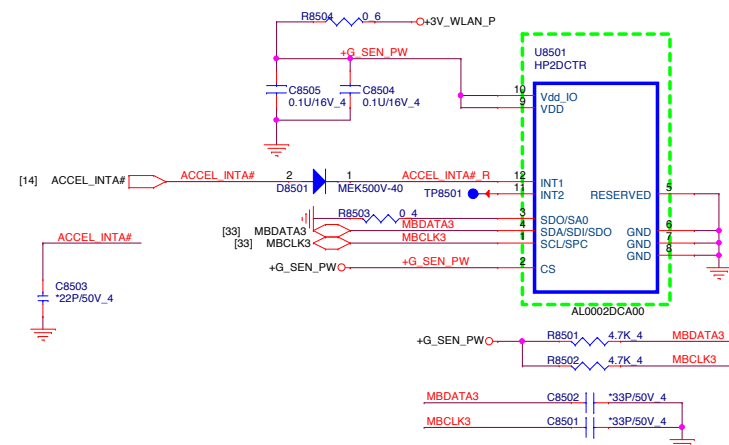


1015 Add IR CAM circuit

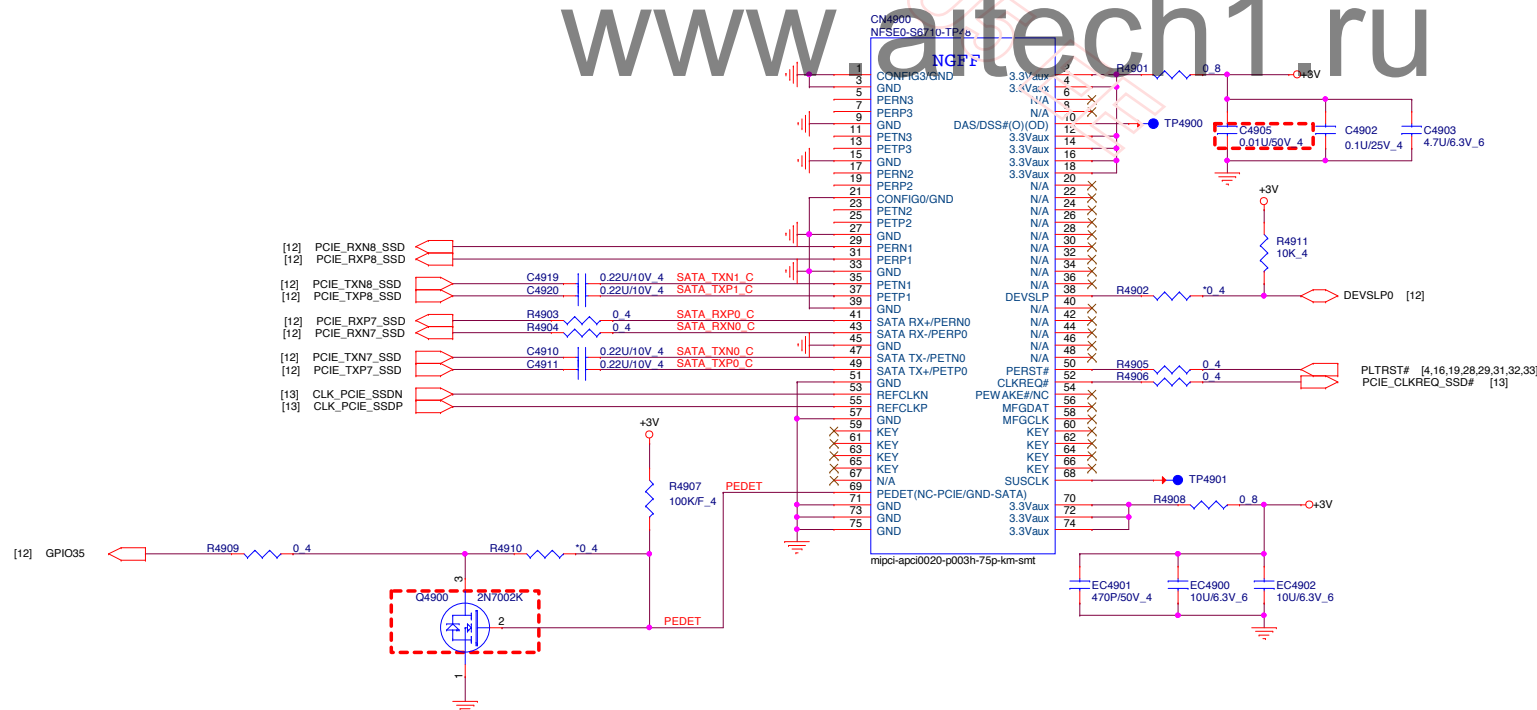
TPM (2.0)



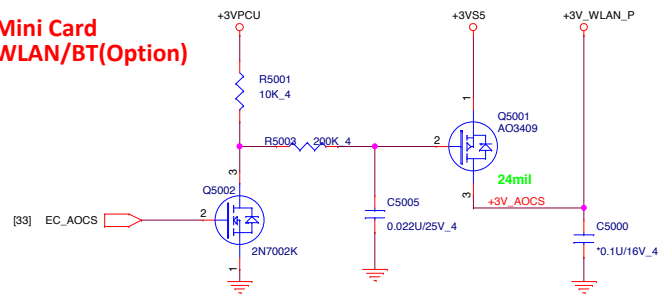
Accelerometer Sensor



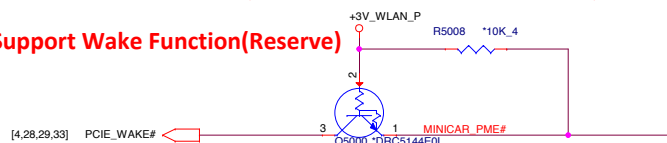
SSD



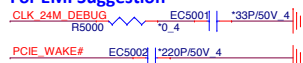
**Mini Card
WLAN/BT(Optional)**



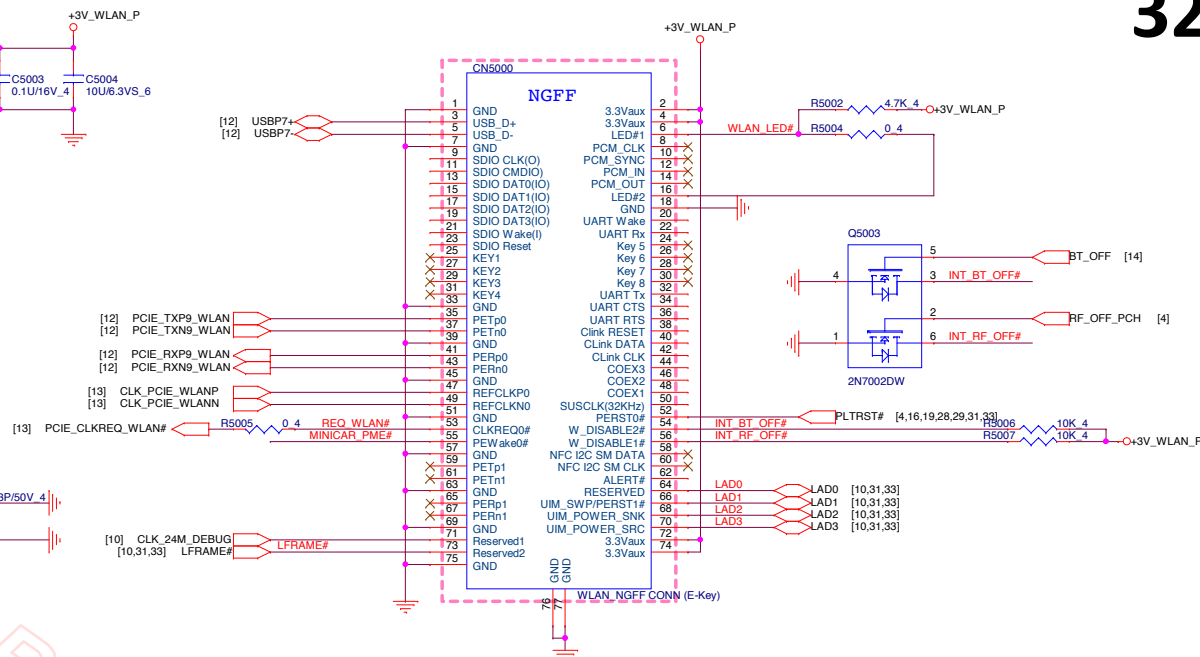
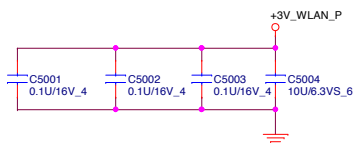
Support Wake Function(Reserve)



For EMI Suggestion

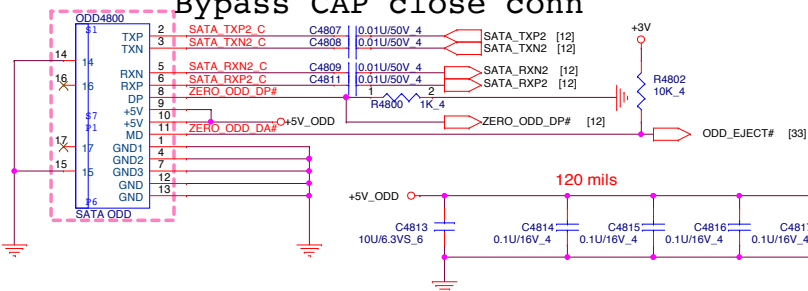


1020 del EC PCIE WAKE# circuit

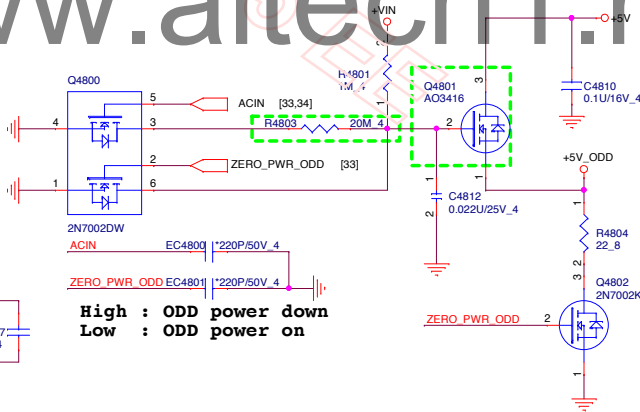
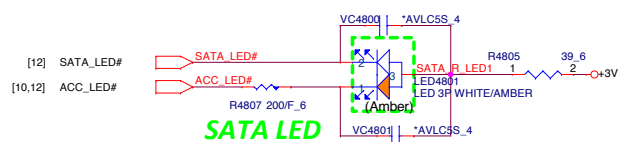
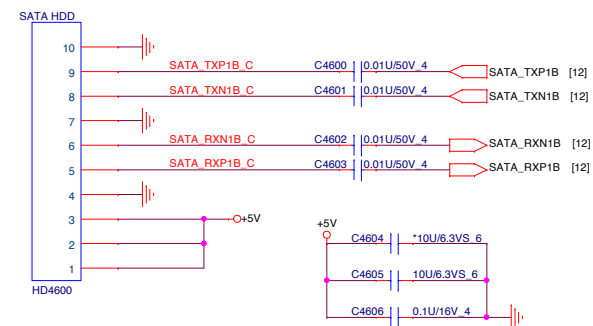


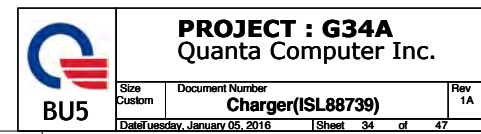
SATA ODD

Bypass CAP close conn



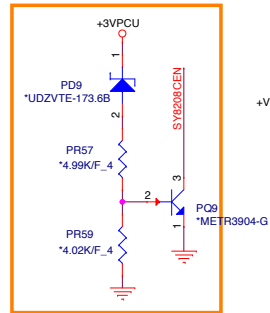
High : ODD power down
Low : ODD power on

**HDD**



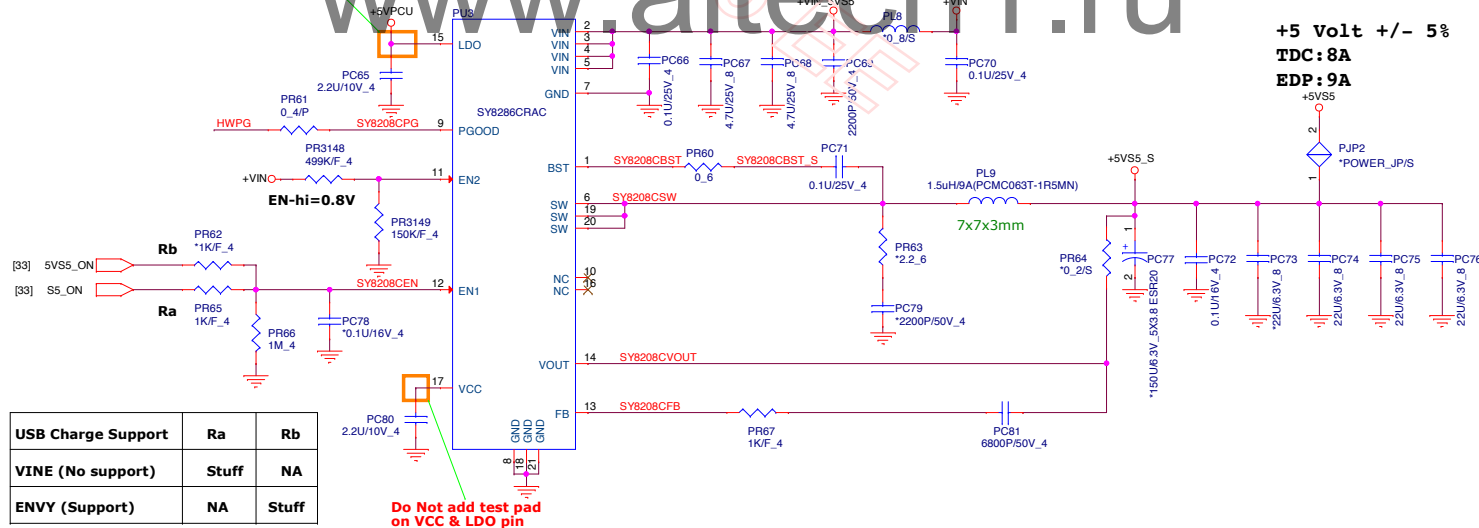
+VIN [25,30,32,34,36,37,39,40,41,42,44,45,47]
 +3VS5 [4,10,15,16,25,32,33,36,37,38,42,43,46,47]
 +5VS5 [4,25,26,29,36,37,38,39,40,41,43,44,45,46]
 +3VPCU [6,13,30,32,33,34,42,47]
 +5VPCU [26,34,43,46]

Do Not add test pad on VCC & LDO pin



2014/12/12 updated

Do Not add test pad on VCC & LDO pin



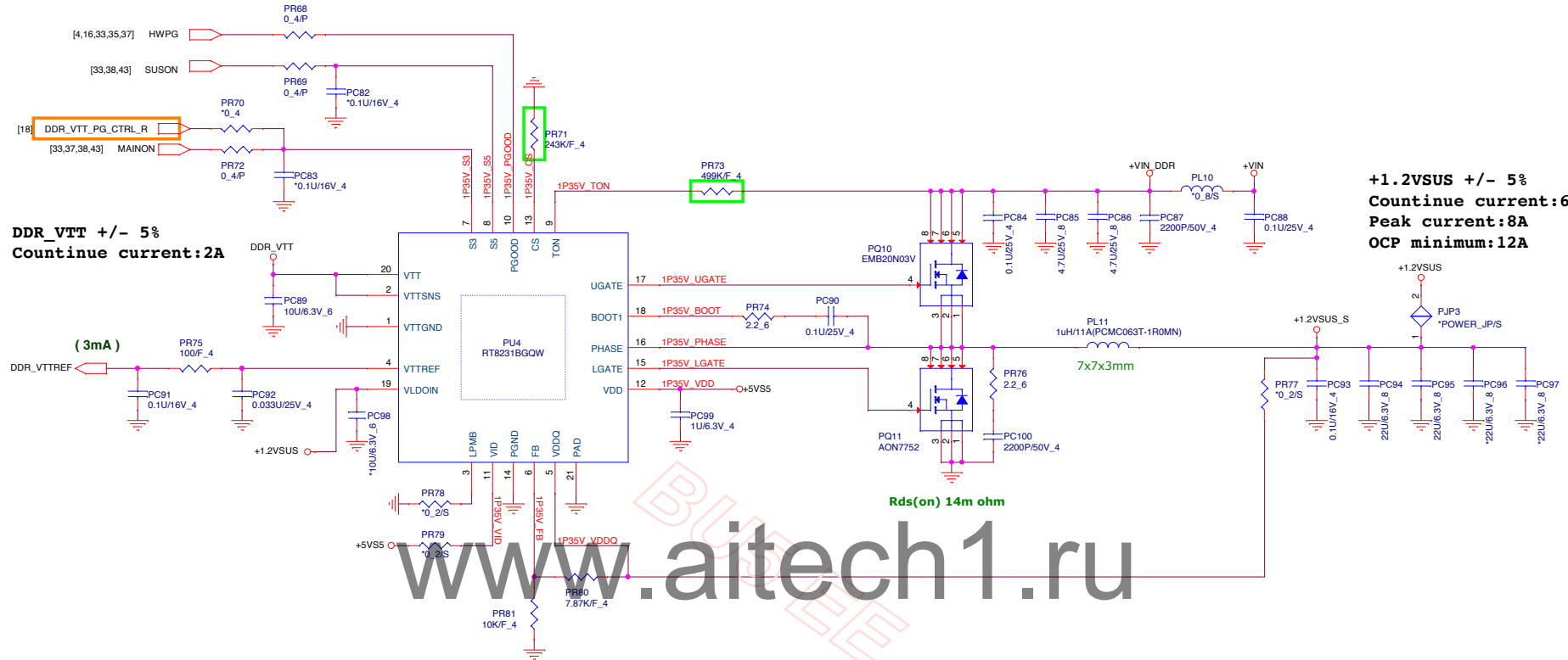
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

Do Not add test pad on VCC & LDO pin

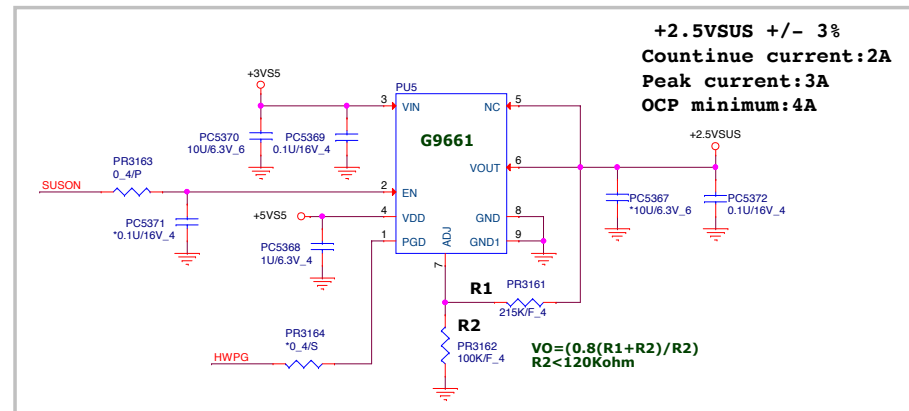
+3.3 Volt +/- 5%
 TDC:8A
 EDP:9A

+5 Volt +/- 5%
 TDC:8A
 EDP:9A

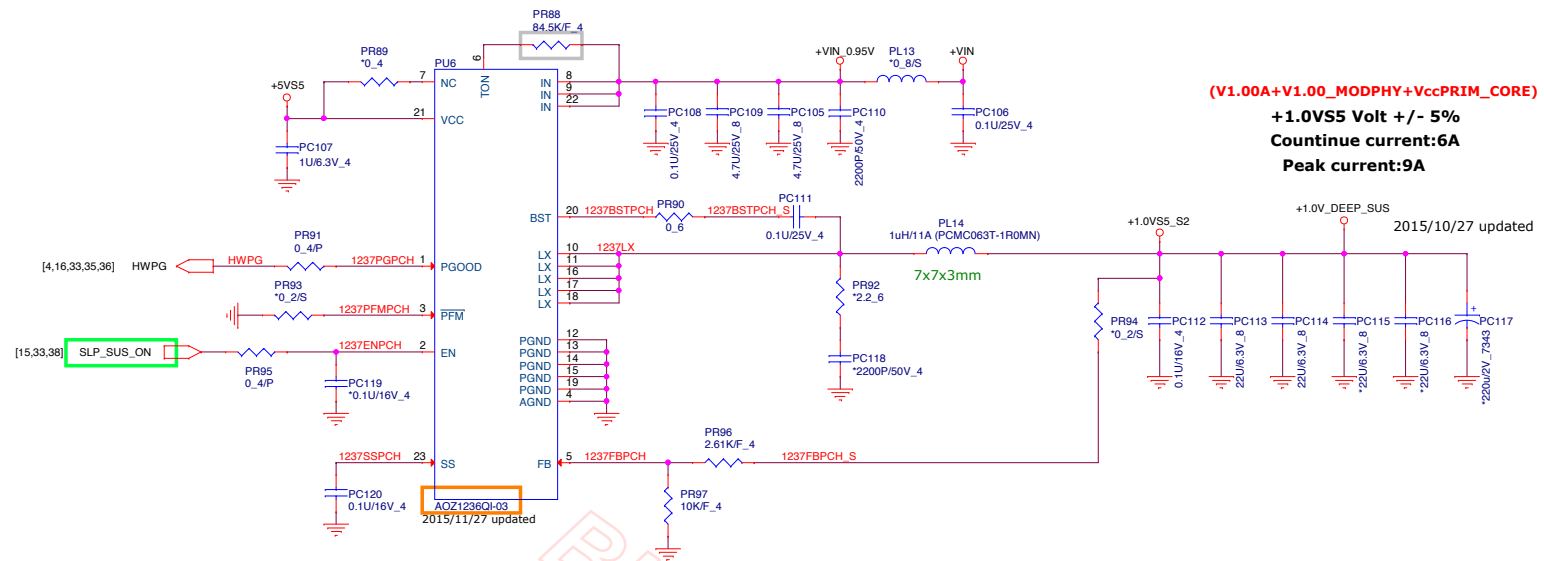
+VIN [25,30,32,34,35,37,39,40,41,42,44,45,47]
 +5VS5 [4,25,26,29,35,37,38,39,40,41,43,44,45,46]
 +1.2VSUS [3,6,17,18,38,46]
 DDR_VTT [17,18]



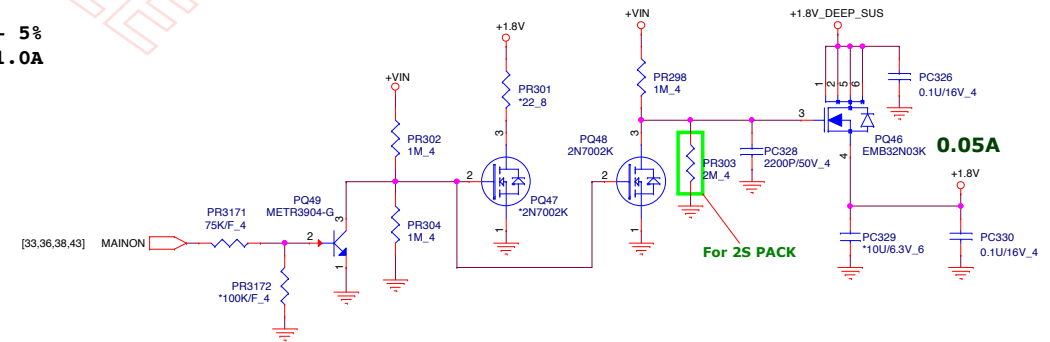
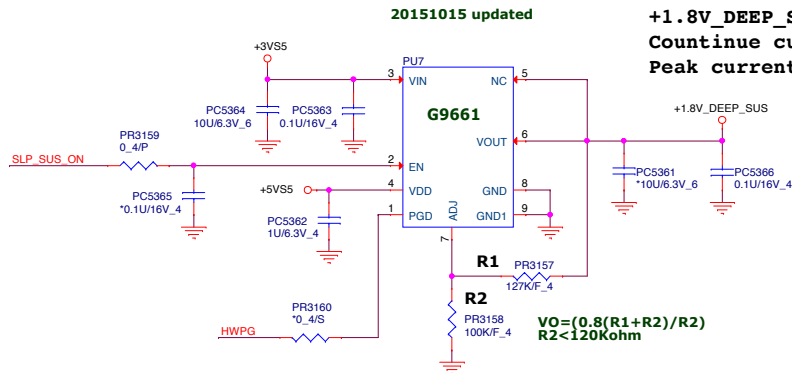
20151015 updated



+VIN	[25,30,32,34,35,36,39,40,41,42,44,45,47]
+3VS5	[4,10,15,16,25,32,33,36,38,42,43,46,47]
+5VS5	[4,25,26,29,35,36,38,39,40,41,43,44,45,46]
+1.0V_DEEP_SUS	[9,13,15,16,38]
+1.8V_DEEP_SUS	[5,9,15,47]
+1.8V	[26]



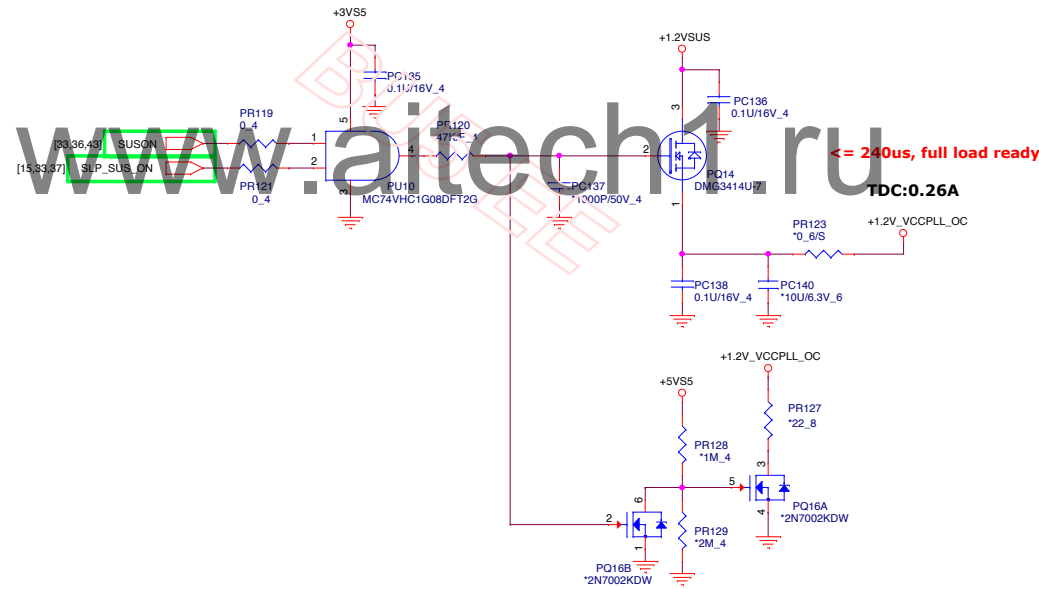
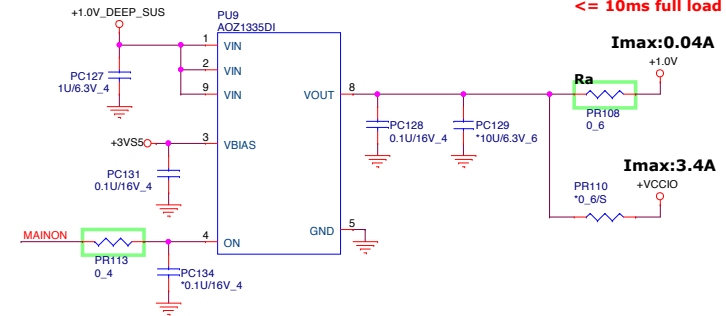
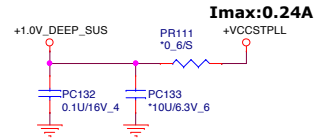
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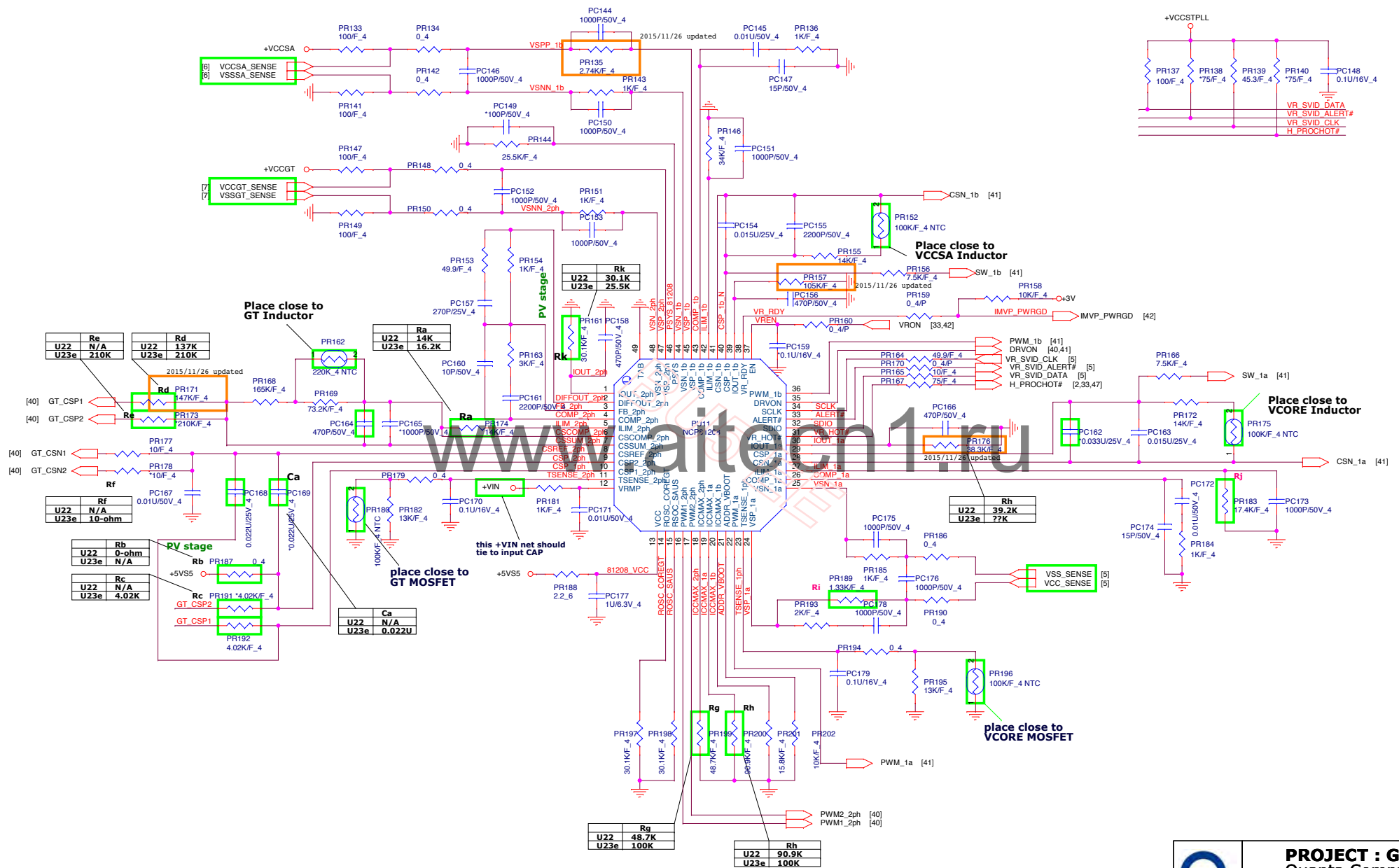
+1.0V [2,4,6,16,33]
 +3VS5 [4,10,15,16,25,32,33,35,36,37,42,43,46,47]
 +5VS5 [4,25,26,29,35,36,37,39,40,41,43,44,45,46]
 +VCCIO [2,6,16]
 +1.2VSUS [3,6,17,18,36,46]
 +VCCSTPLL [2,4,5,6,9,39]
 +1.0V_DEEP_SUS [9,13,15,16,37]
 +1.2V_VCCPLL_OC [6]
 MAINON [33,36,37,43]

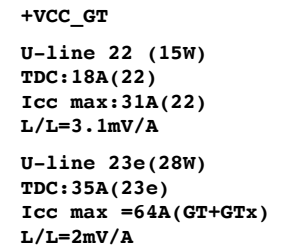
Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
 (Vcc_ST+Vcc_PLL)

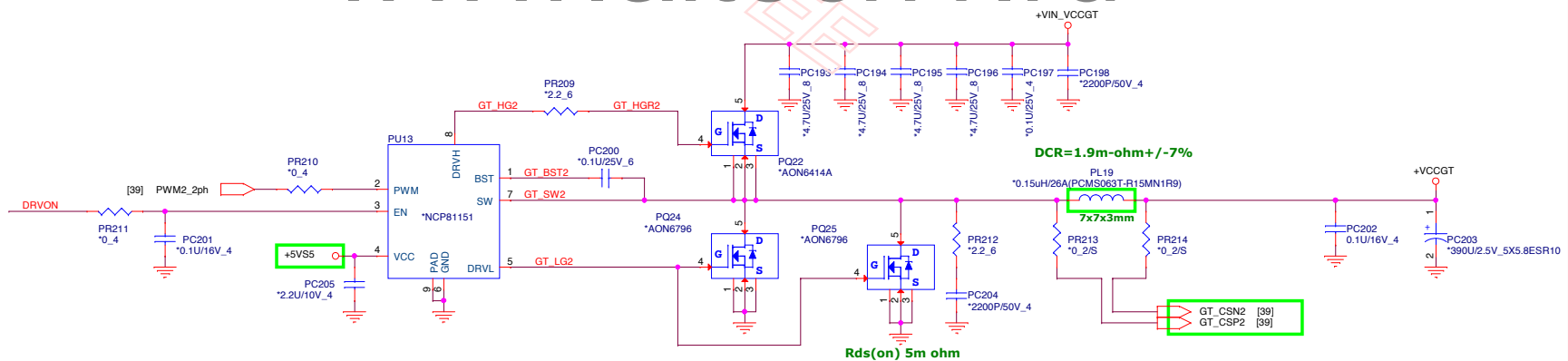


+3V [2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,43,44,47]
 +5V [25,26,27,30,32,43]
 +VIN [25,30,32,34,35,36,37,40,41,42,44,45,47]
 +5VPCU [26,34,35,43,46]
 +VCCSA [6,41]
 +VCCGT [7,40]
 +VCCSTPLL [2,4,5,6,9,38]

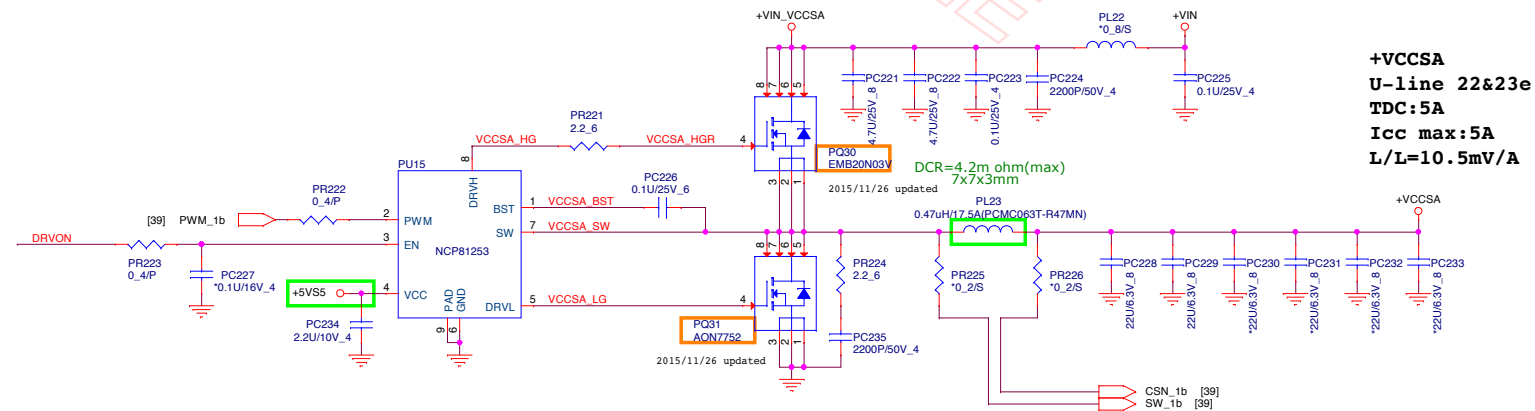
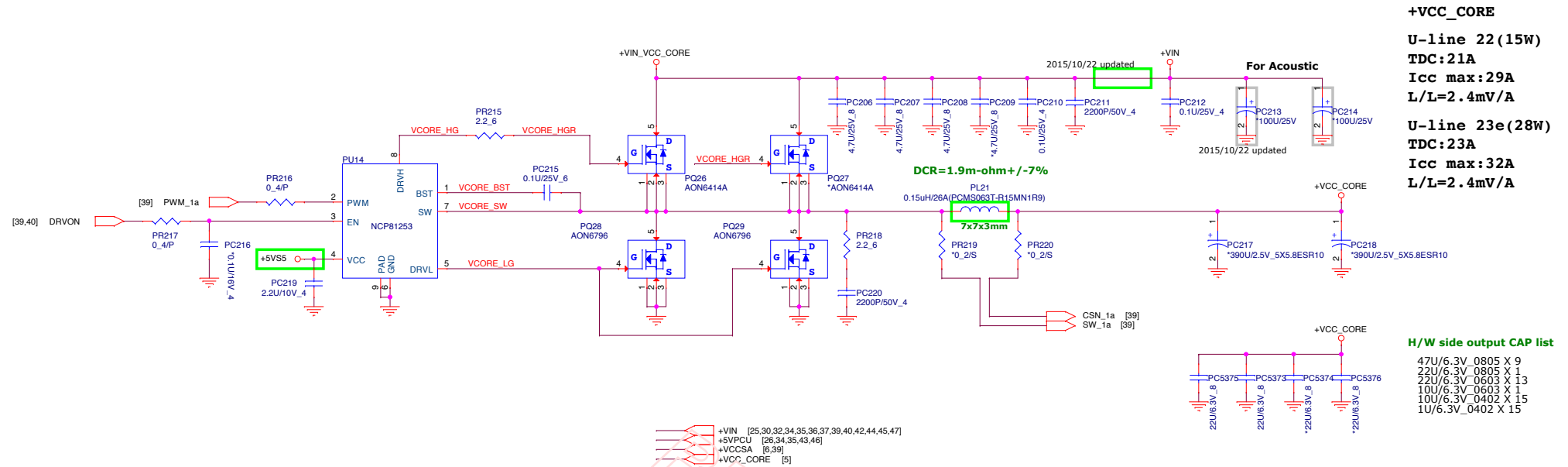




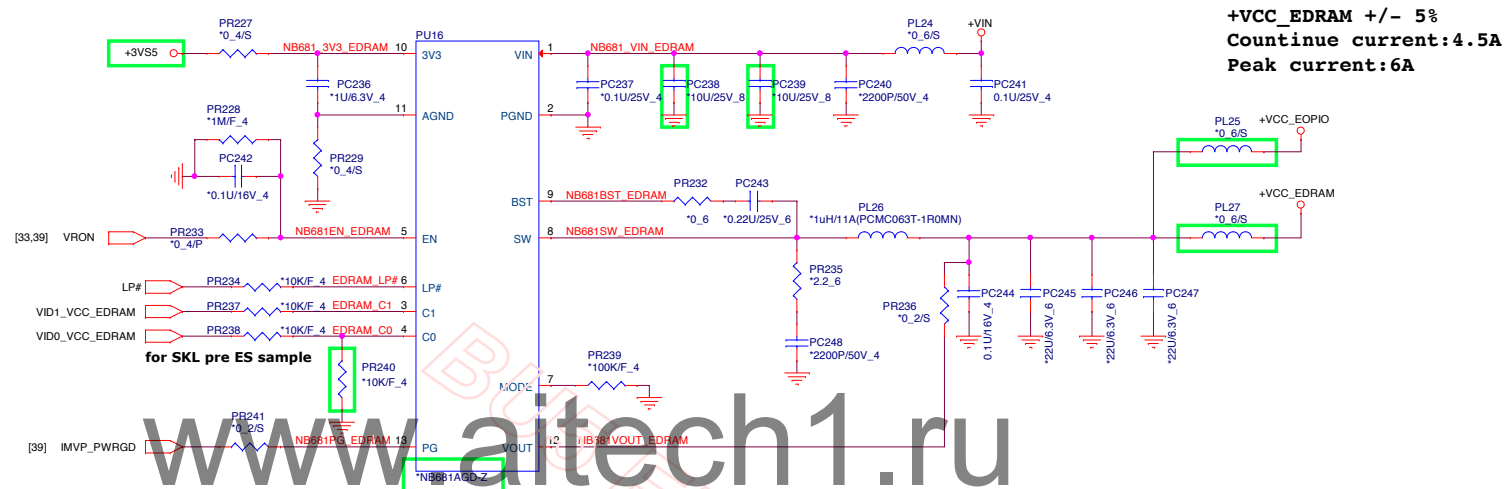
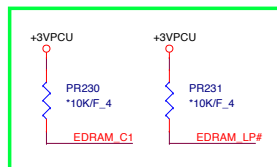
Components



Size Custom	Document Number +VCCSA (NCP81253)	Rev 2A
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+VIN [25,30,32,34,35,36,37,39,40,41,44,45,47]
 +3VPCU [6,13,30,32,33,34,35,47]
 +VCC_EOPIO [5]
 +VCC_EDRAM [5]



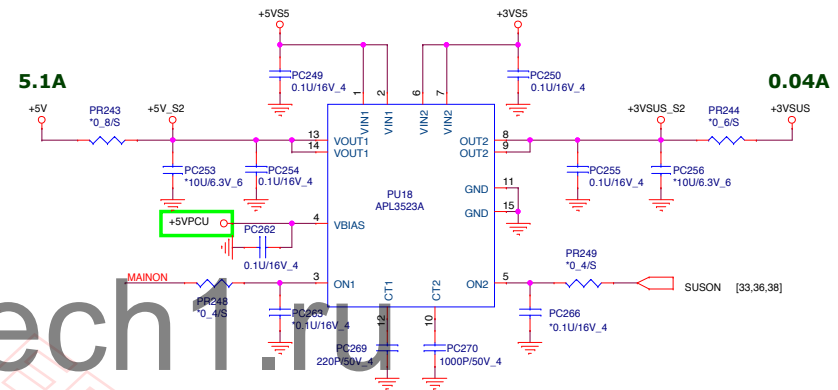
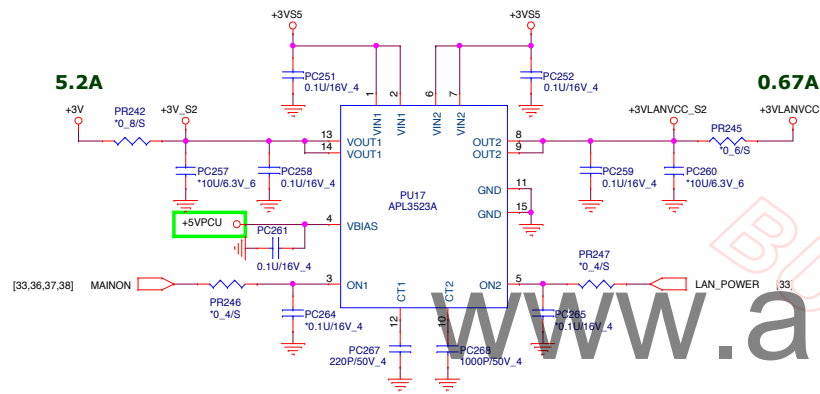
VCC_EDRAM

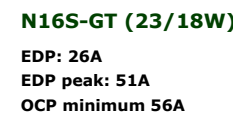
LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

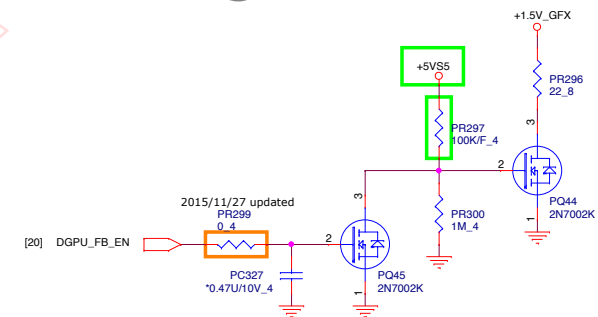
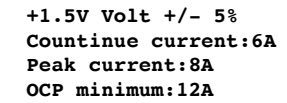
MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

+3V	[2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,44,47]
+5V	[25,26,27,30,32]
+VIN	[25,30,32,34,35,36,37,39,40,41,42,44,45,47]
+3VS5	[4,10,15,16,25,32,33,35,36,37,38,42,46,47]
+5VS5	[4,25,26,29,35,36,37,38,39,40,41,44,45,46]
+3VSUS	[30]
+5V_CAM	
+3VLAVCC	[28]







+VIN [25,30,32,34,35,36,37,39,40,41,42,44,45,47]
 +3VS5 [4,10,15,16,25,32,33,35,36,37,38,42,43,47]
 +5VS5 [4,25,26,29,35,36,37,38,39,40,41,43,44,45]
 +3V_GFX [19,21,22,44,45]
 +3V_AON [19,22]
 +1.2VSUS [3,6,17,18,36,38]
 +1.05V_GFX [19,20,21]

